

Figure 1 consists of two schematic diagrams, (a) and (b), illustrating a GaAs-based semiconductor device.

(a) Top view: A central region 15 is labeled as  $\text{Ga}_{0.5}\text{In}_{0.39}\text{As}$  TQW. It is surrounded by regions 13, 14, 16, and 17. Region 15 is further divided into sub-regions 15R and 15F. Region 13 is labeled as GaAs.

(b) Cross-sectional view: The device structure is shown with layers 11, 12, 13, 14, 15, 16, and 17. Layer 11 is  $n\text{-GaAs}$ . Layer 12 is  $\text{AlAs/GaAs}$ . Layer 13 is  $\text{GaAs}$ . Layer 14 is  $\text{Al}_{0.9}\text{Ga}_{0.1}\text{As/GaAs}$ . Layer 15 is  $\text{Ga}_{0.5}\text{In}_{0.5}\text{P}$ . Layer 16 is  $\text{GaAs}$ . Layer 17 is  $\text{Al}_{0.9}\text{Ga}_{0.1}\text{As/GaAs}$ . A current density  $J$  is indicated by an arrow pointing upwards.

FIG. 2

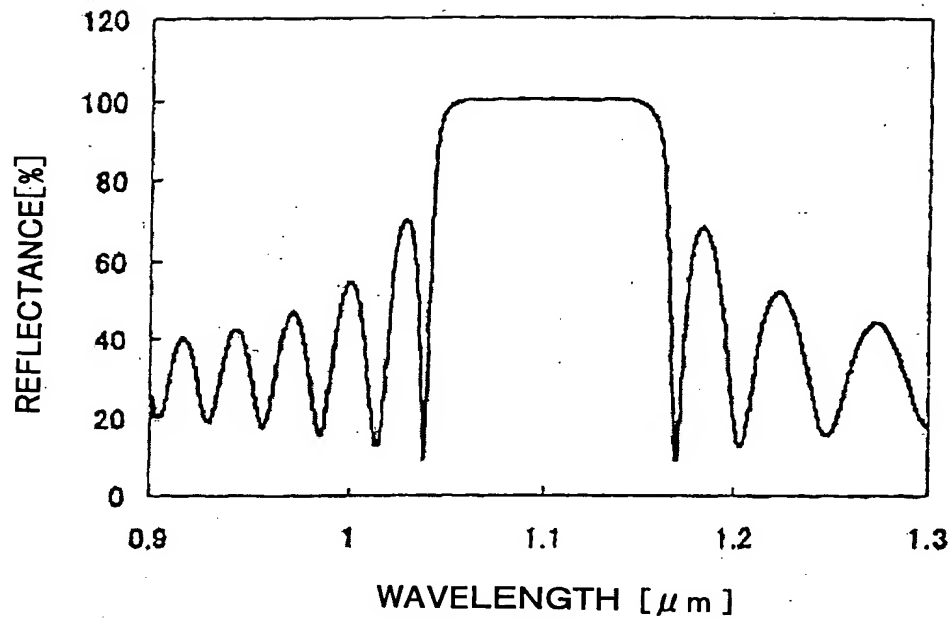


FIG. 3

18 (12)

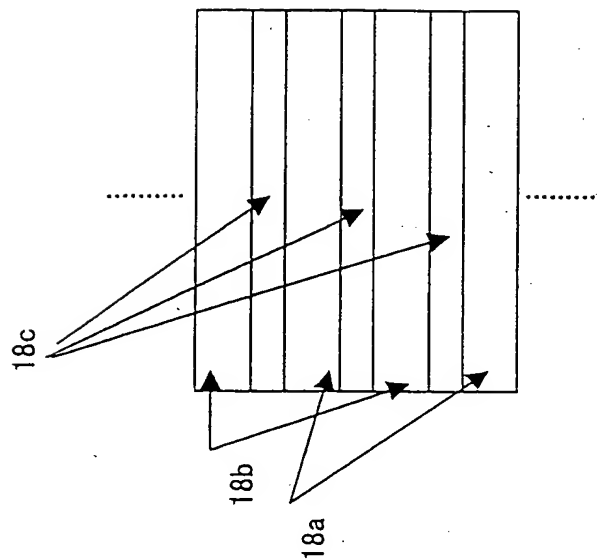


FIG. 4

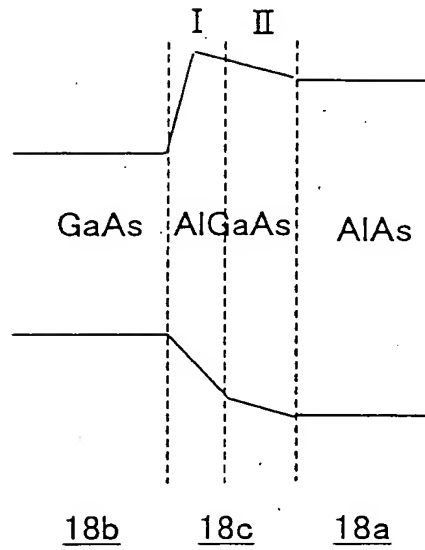
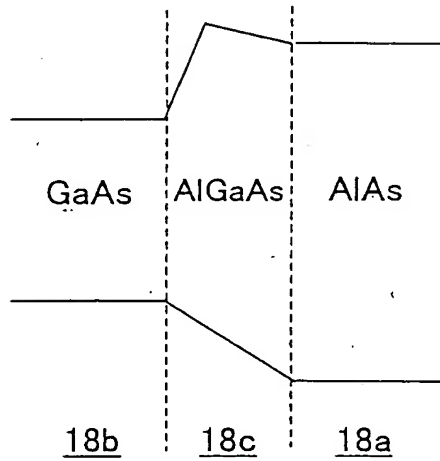


FIG. 5



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FIG. 6

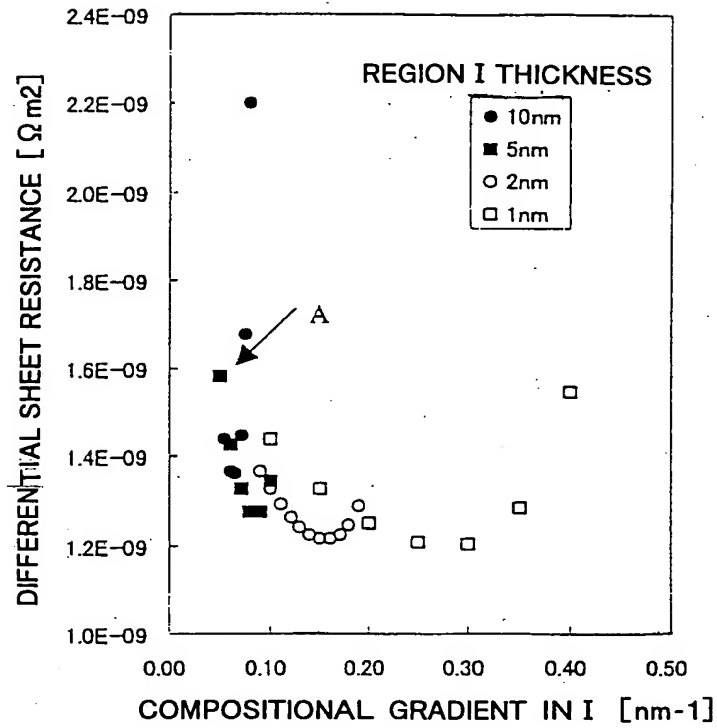


FIG. 7

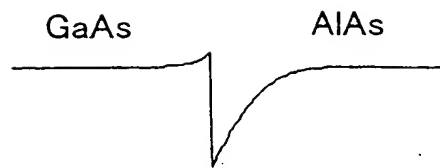


FIG. 8



FIG. 9

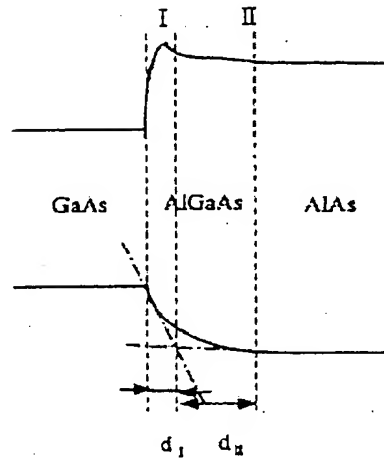


FIG. 10

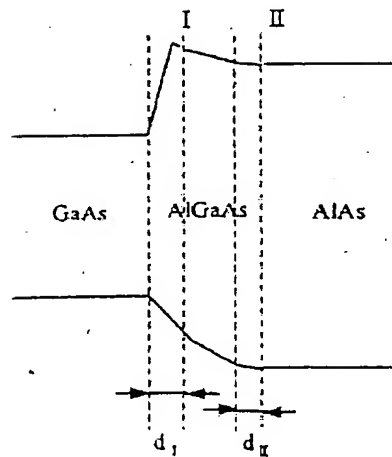




FIG. 11

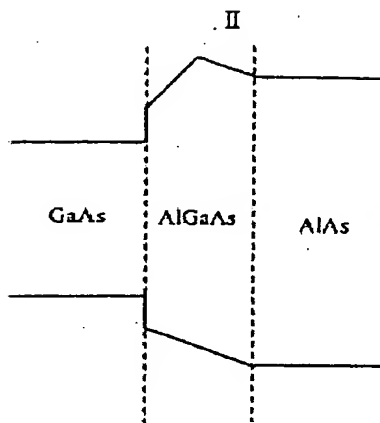


FIG. 12

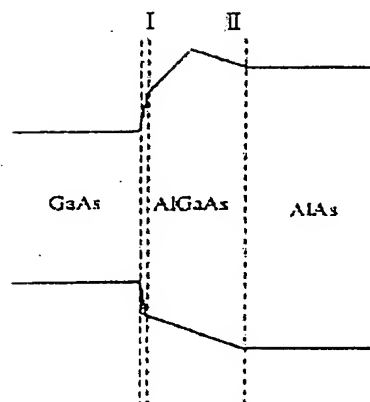


FIG. 13

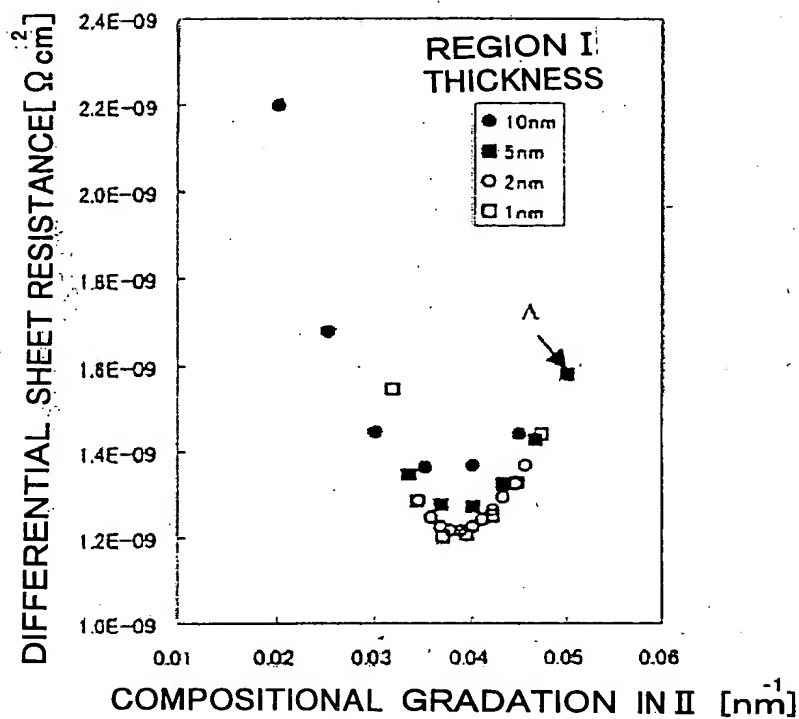


FIG. 14

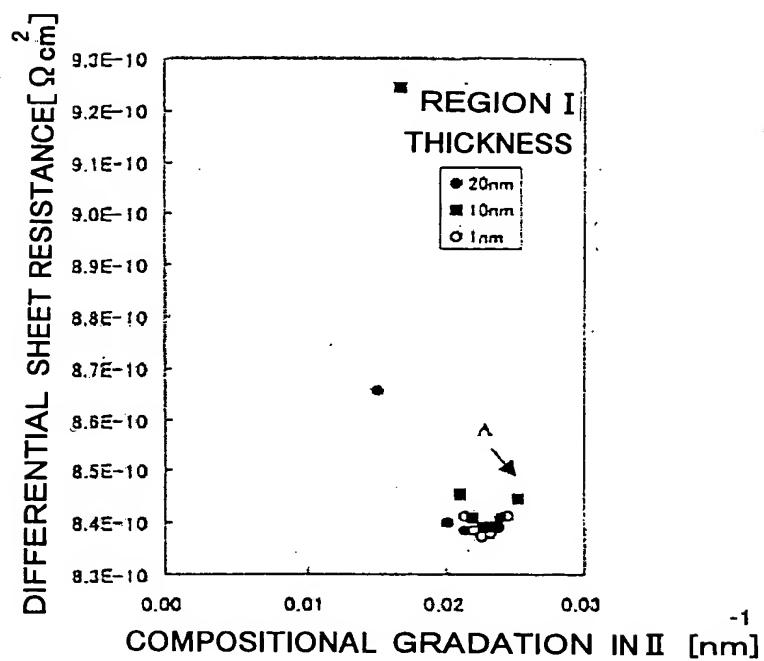


FIG. 15

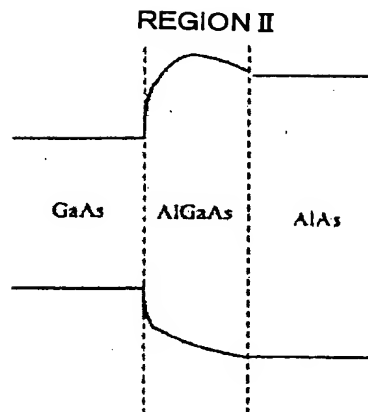


FIG. 16

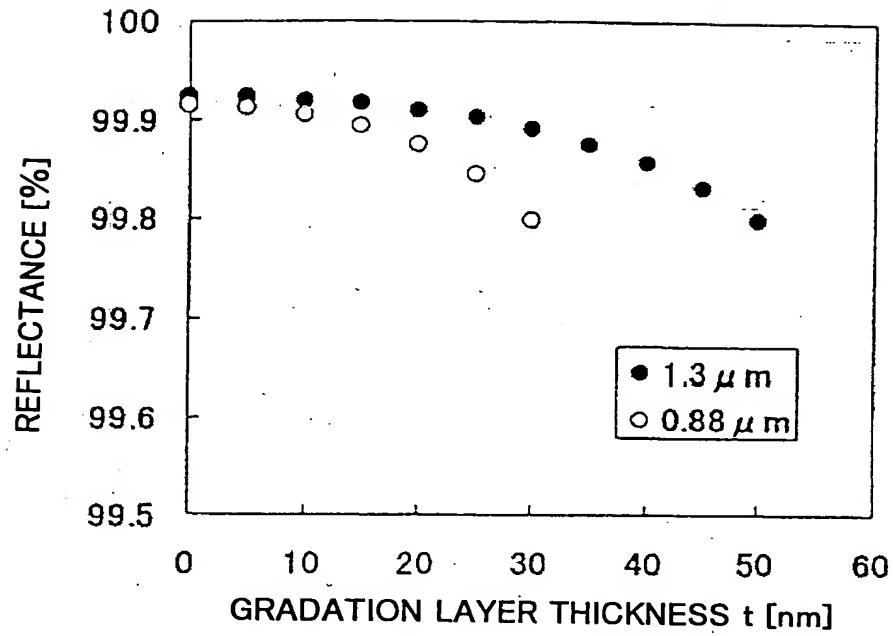


FIG. 17

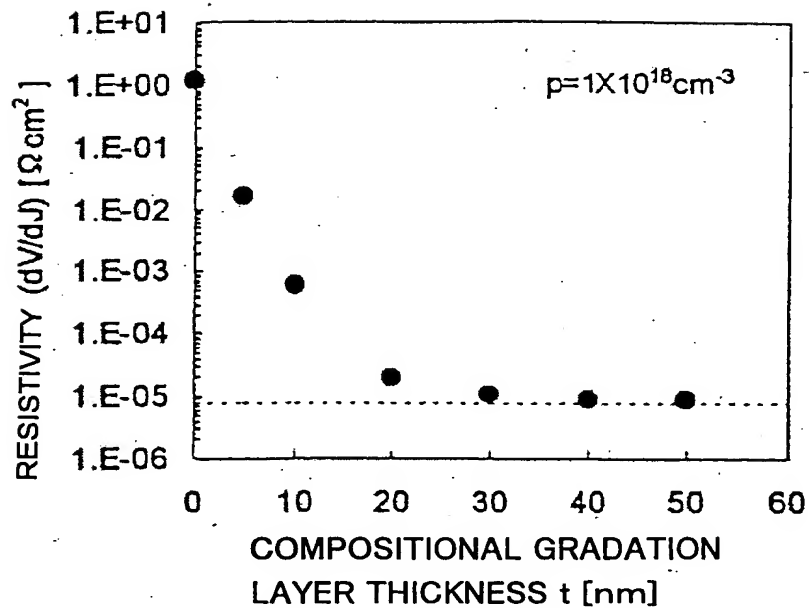


FIG. 18

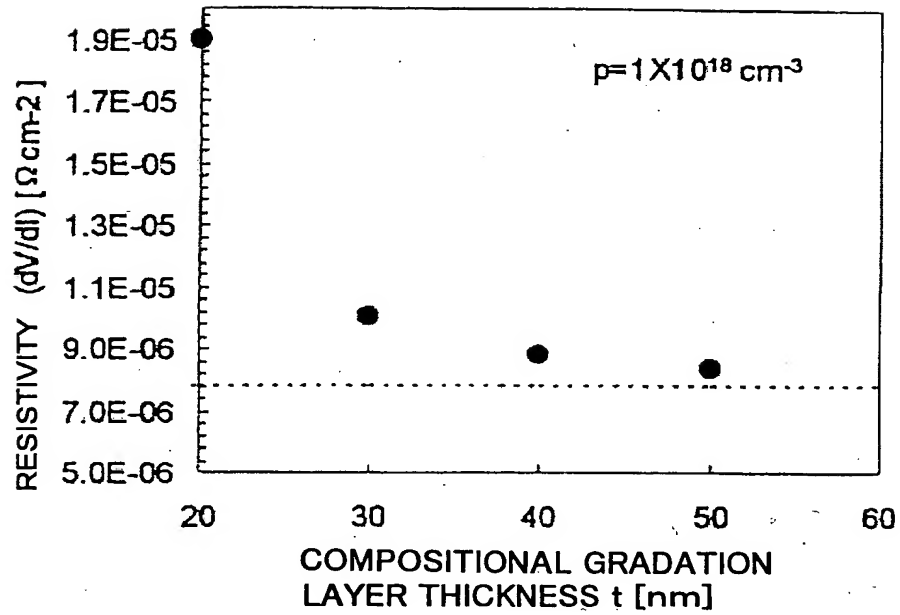


FIG. 19

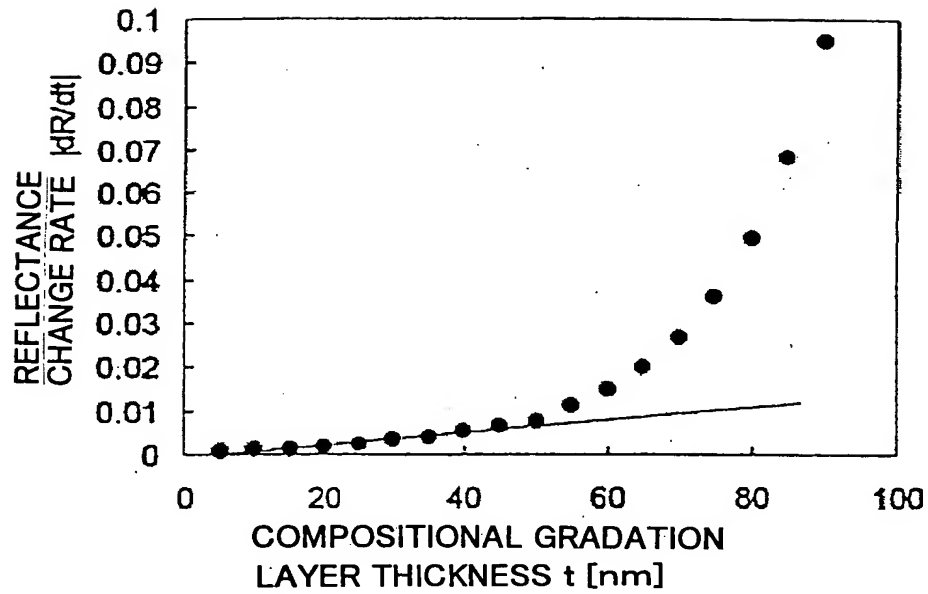




FIG. 20

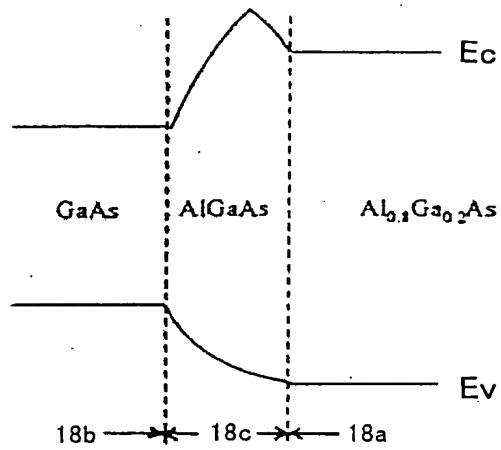


FIG. 21

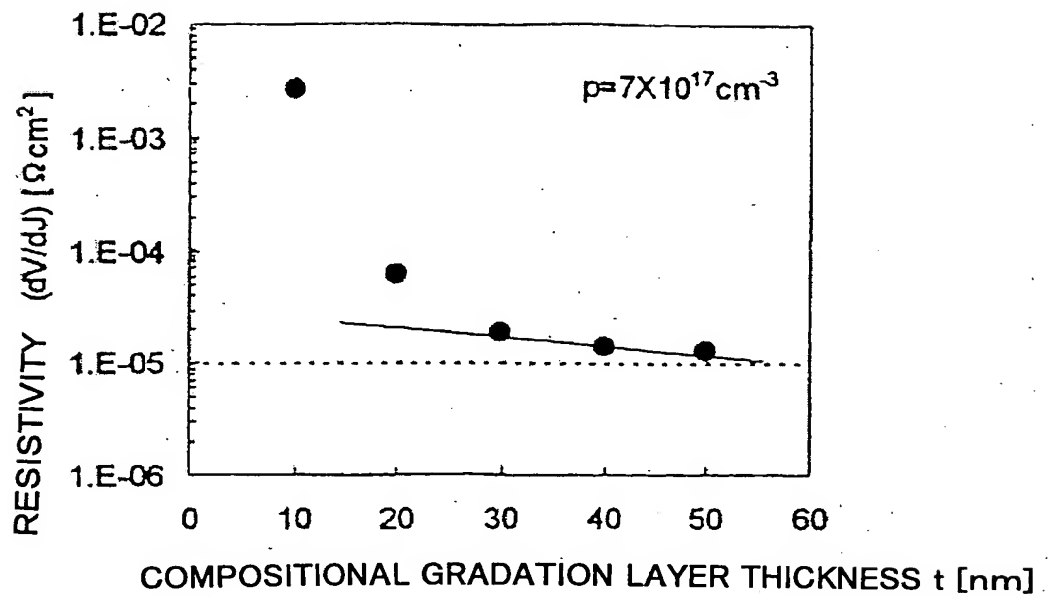


FIG. 22

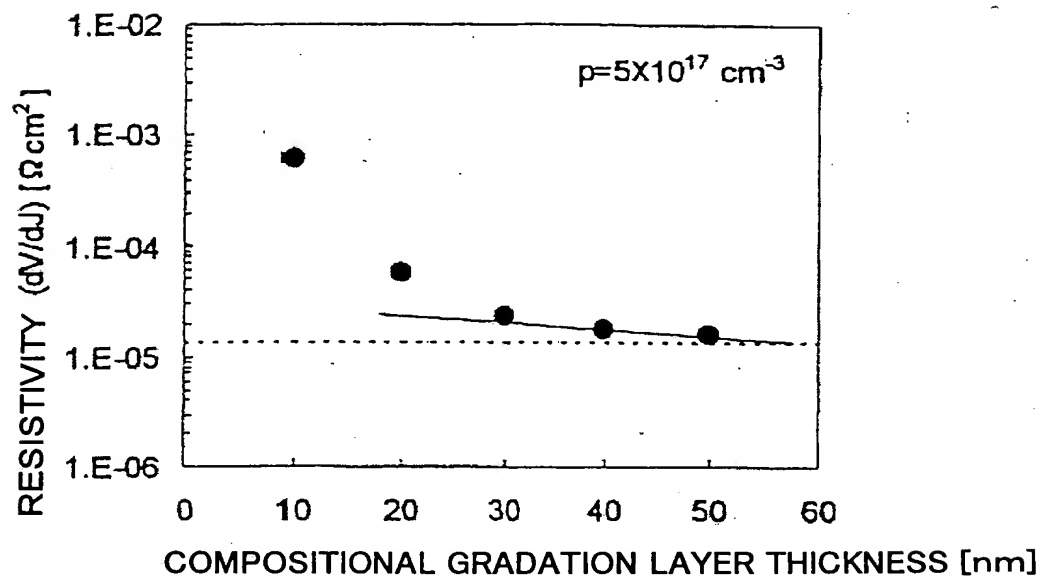


FIG. 23

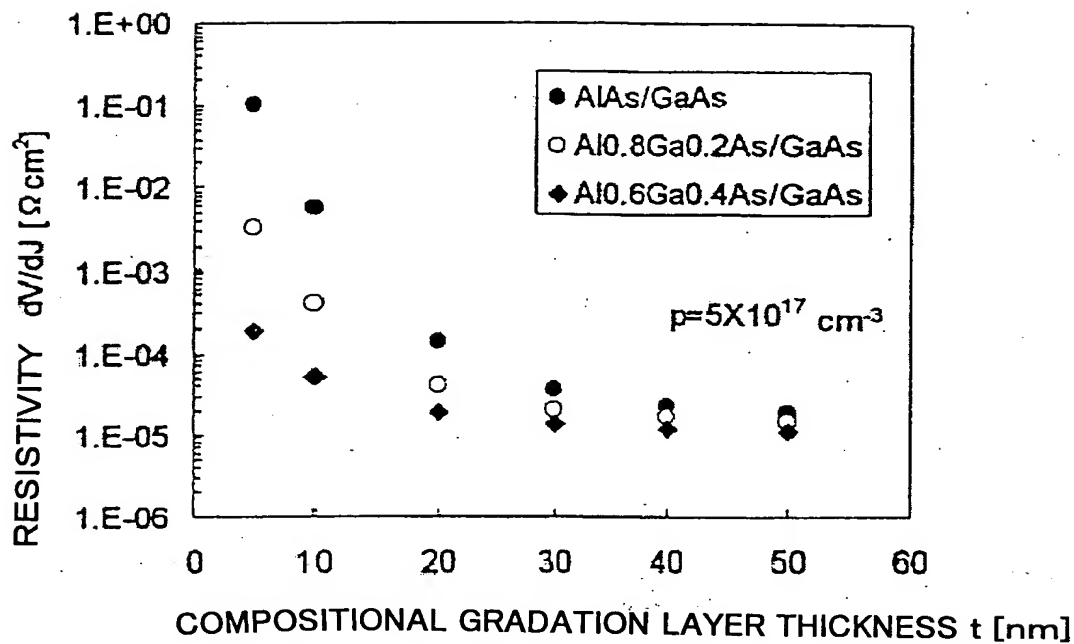


FIG. 24

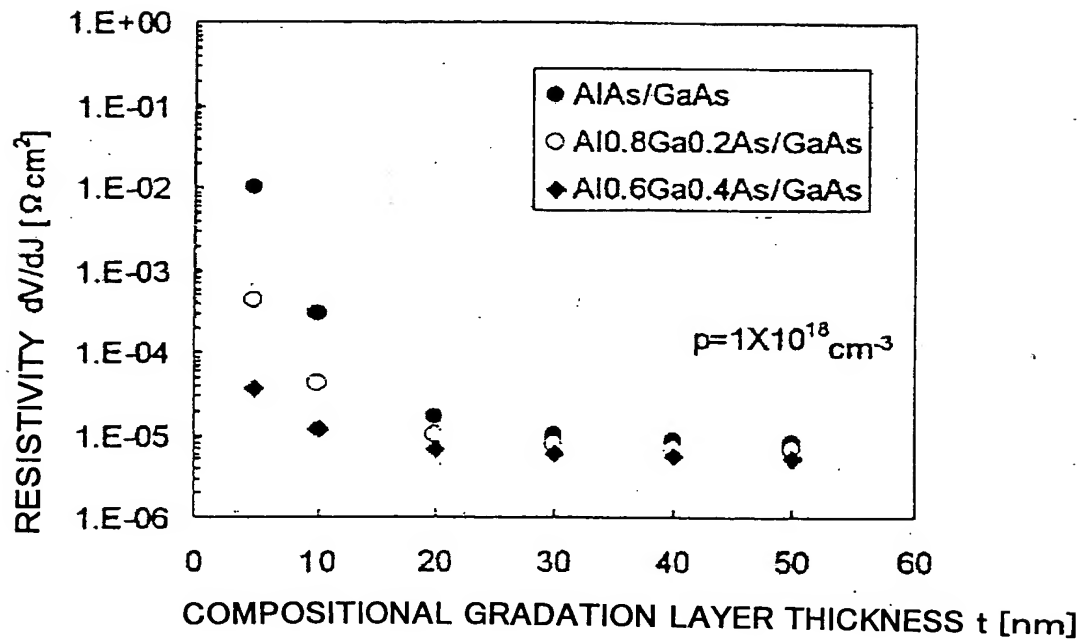


FIG. 25

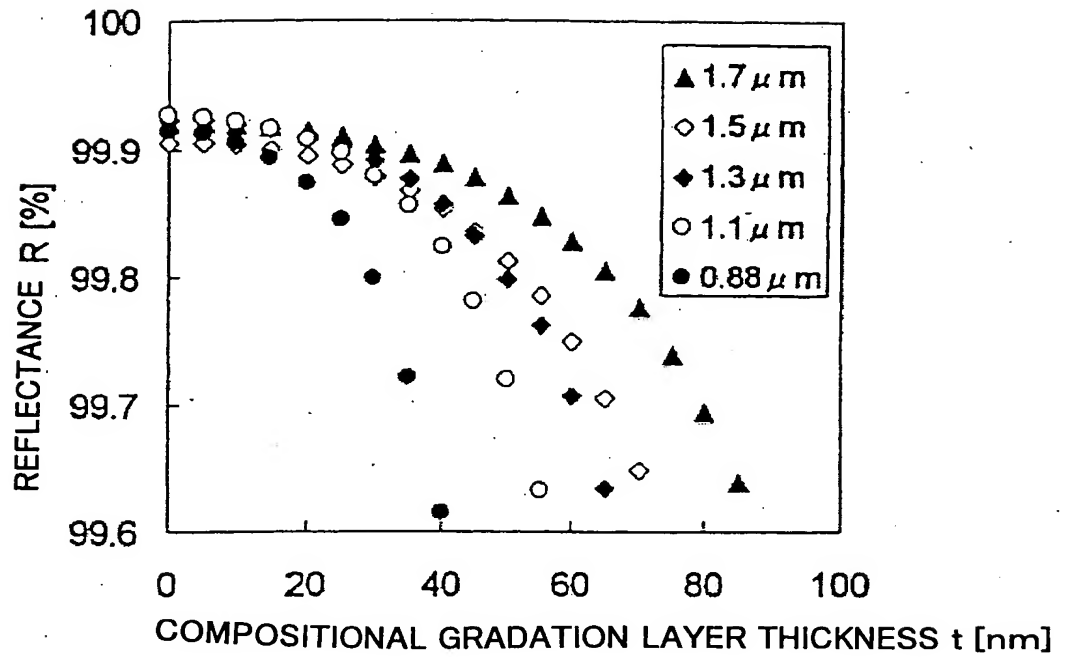


FIG. 26

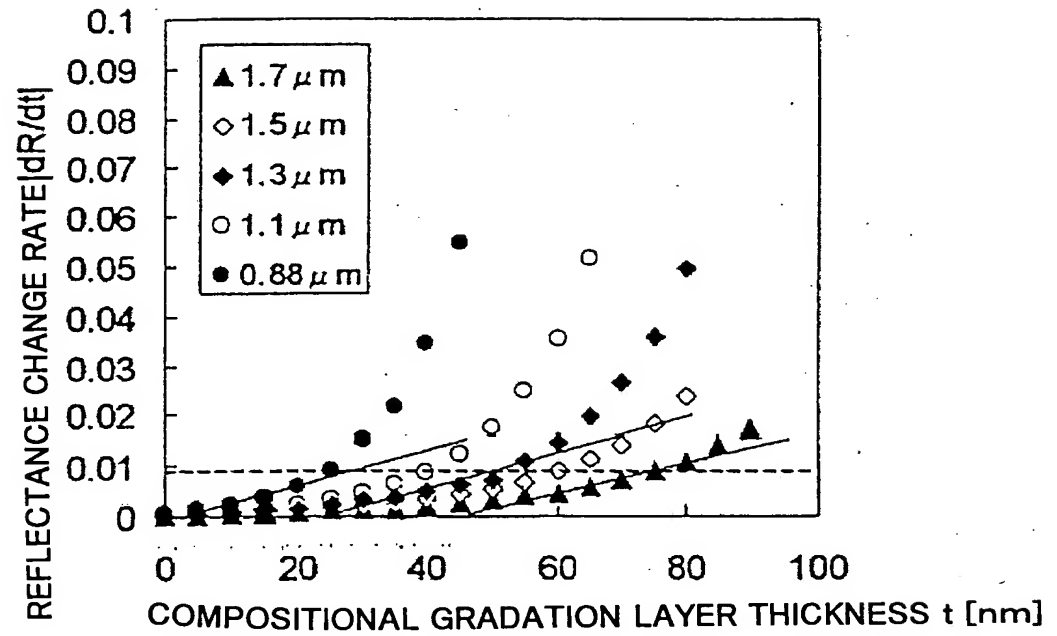


FIG. 27

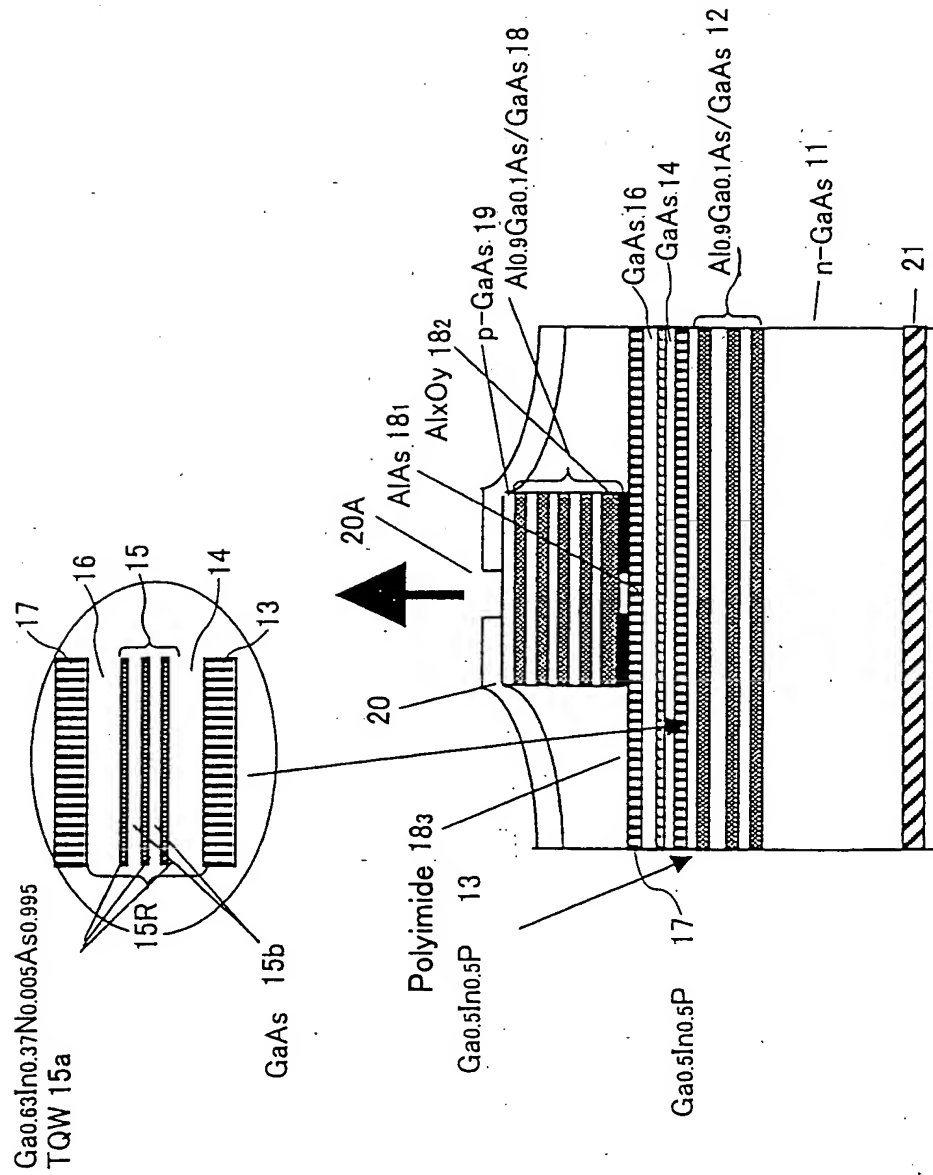




FIG. 28

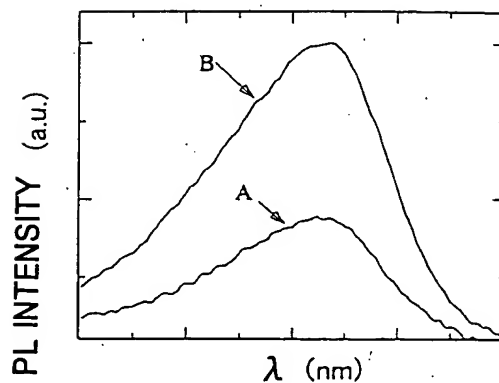
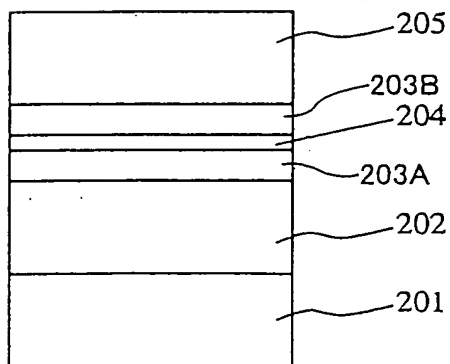


FIG. 29



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FIG. 30

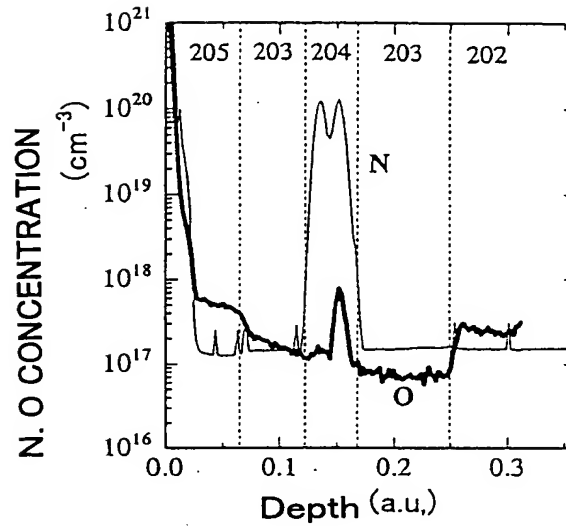


FIG. 31

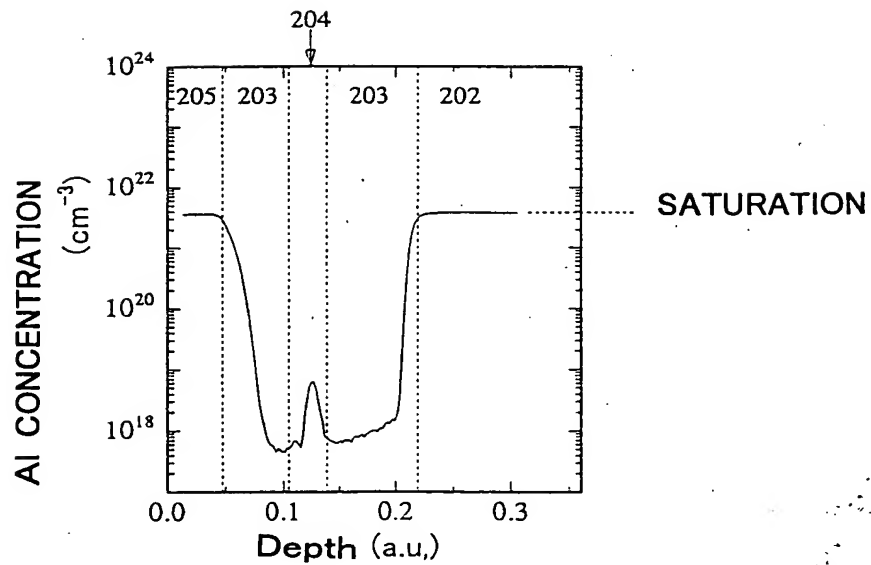


FIG. 32

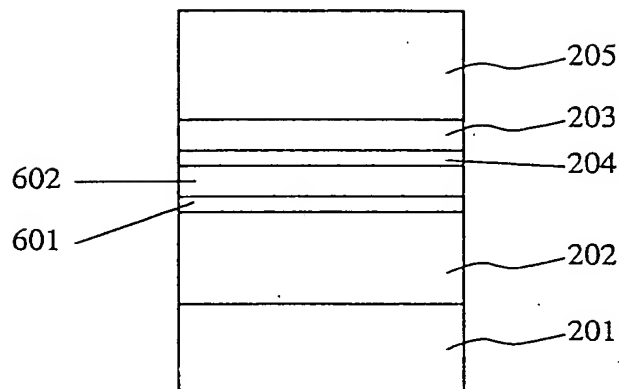


FIG. 33

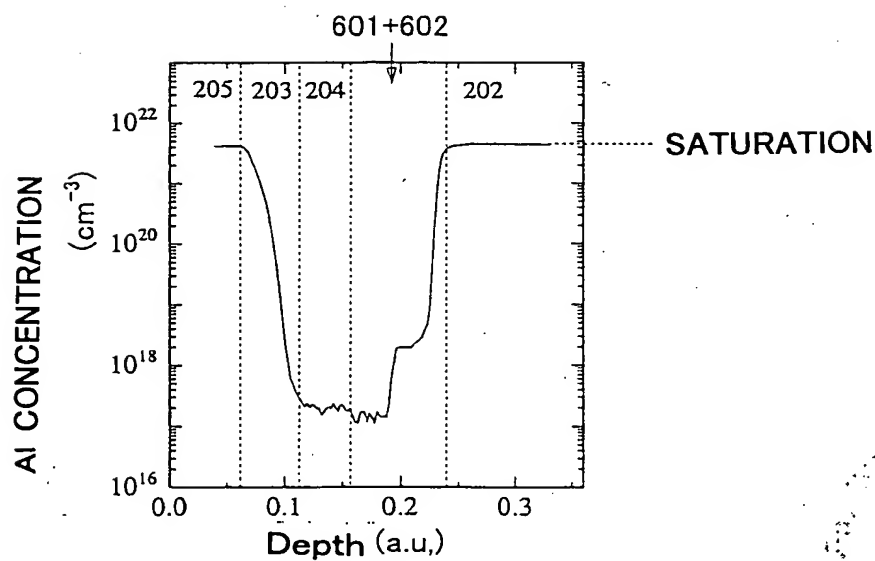


FIG. 34

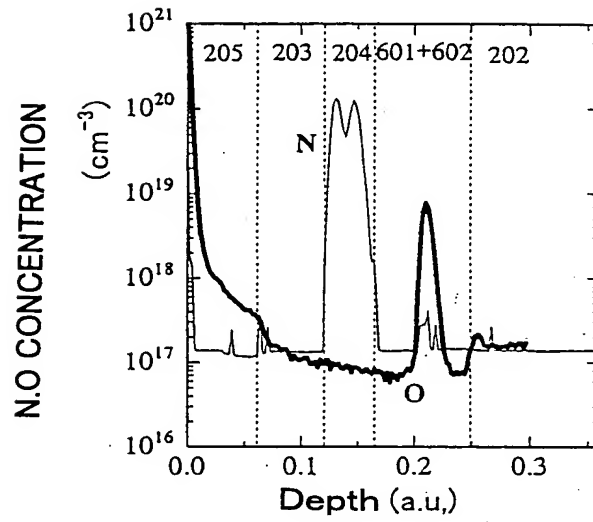


FIG. 35

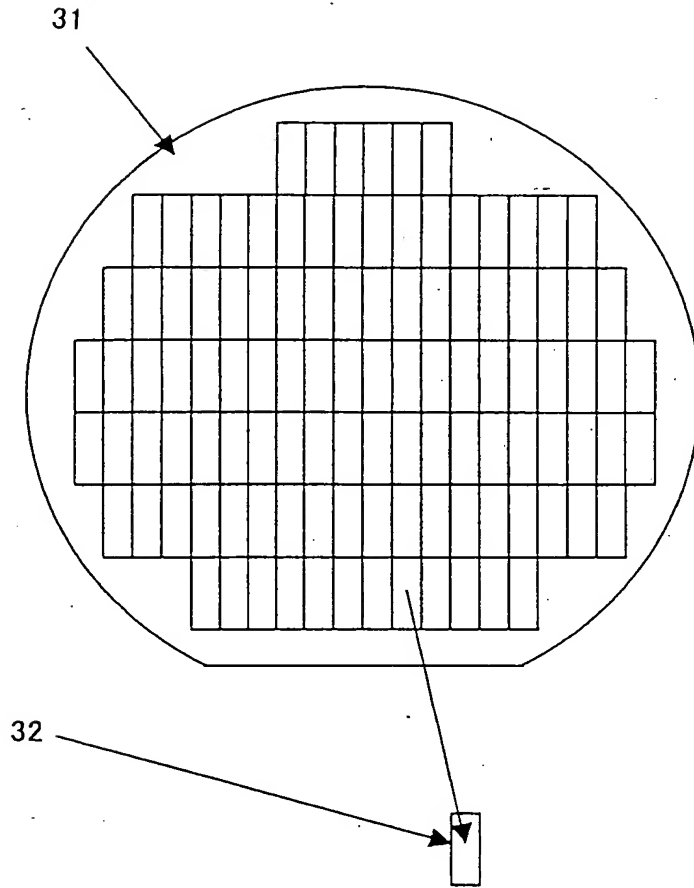


FIG. 36

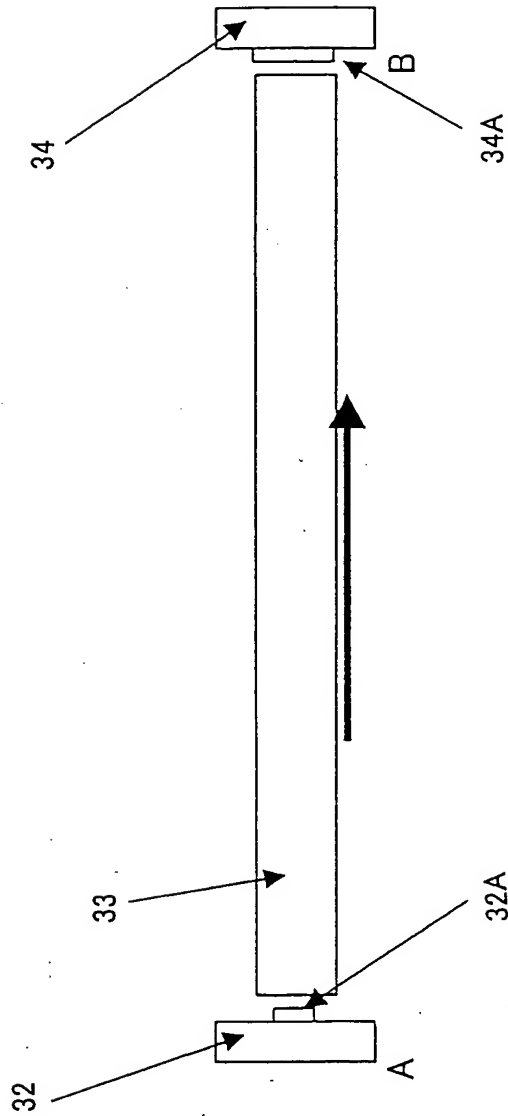


FIG. 37

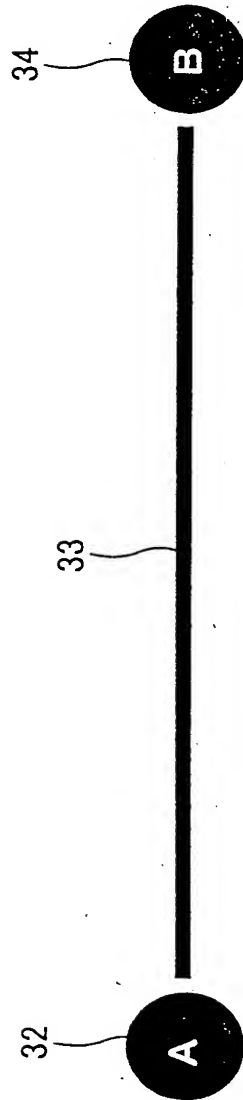


FIG. 38

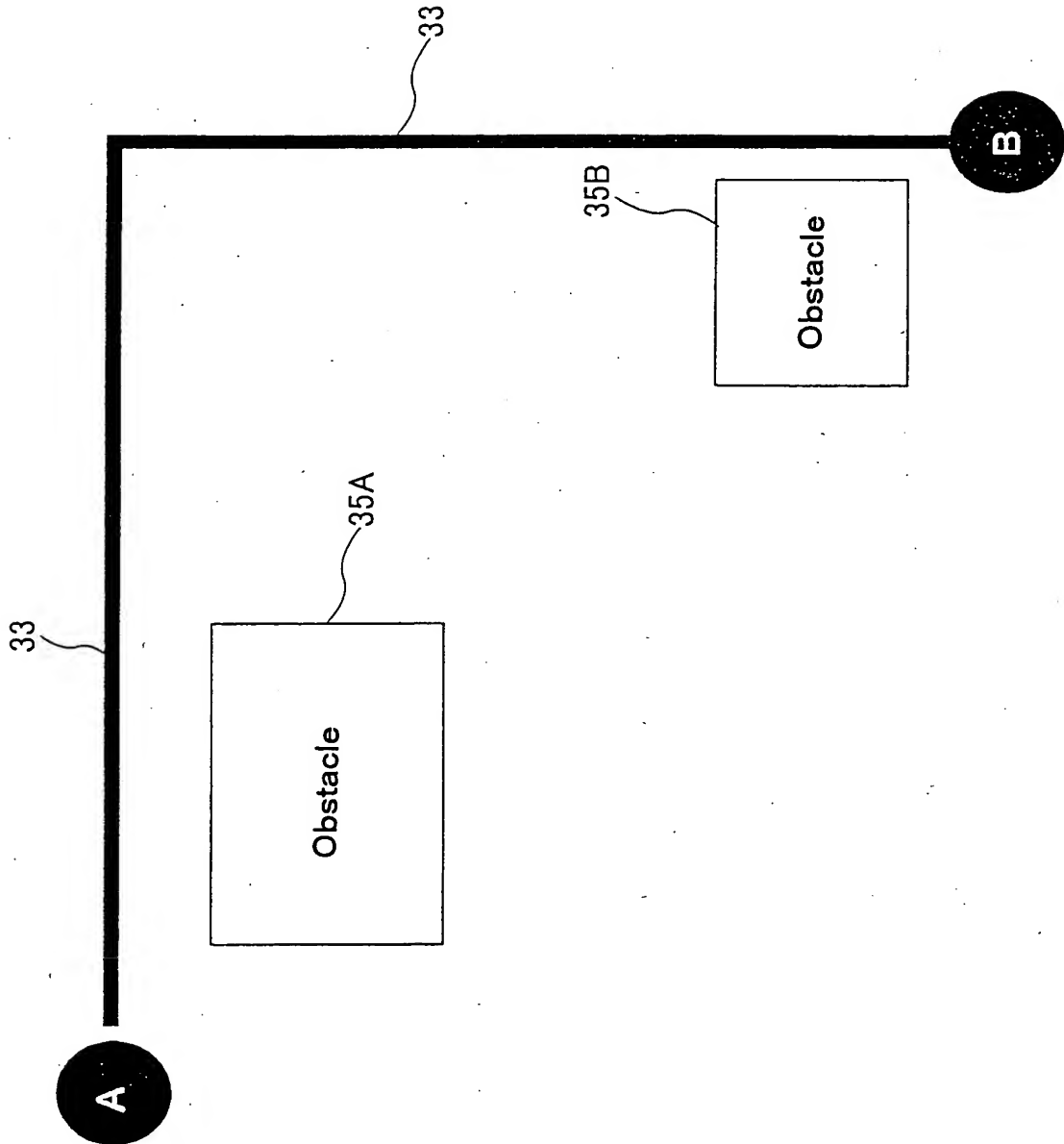
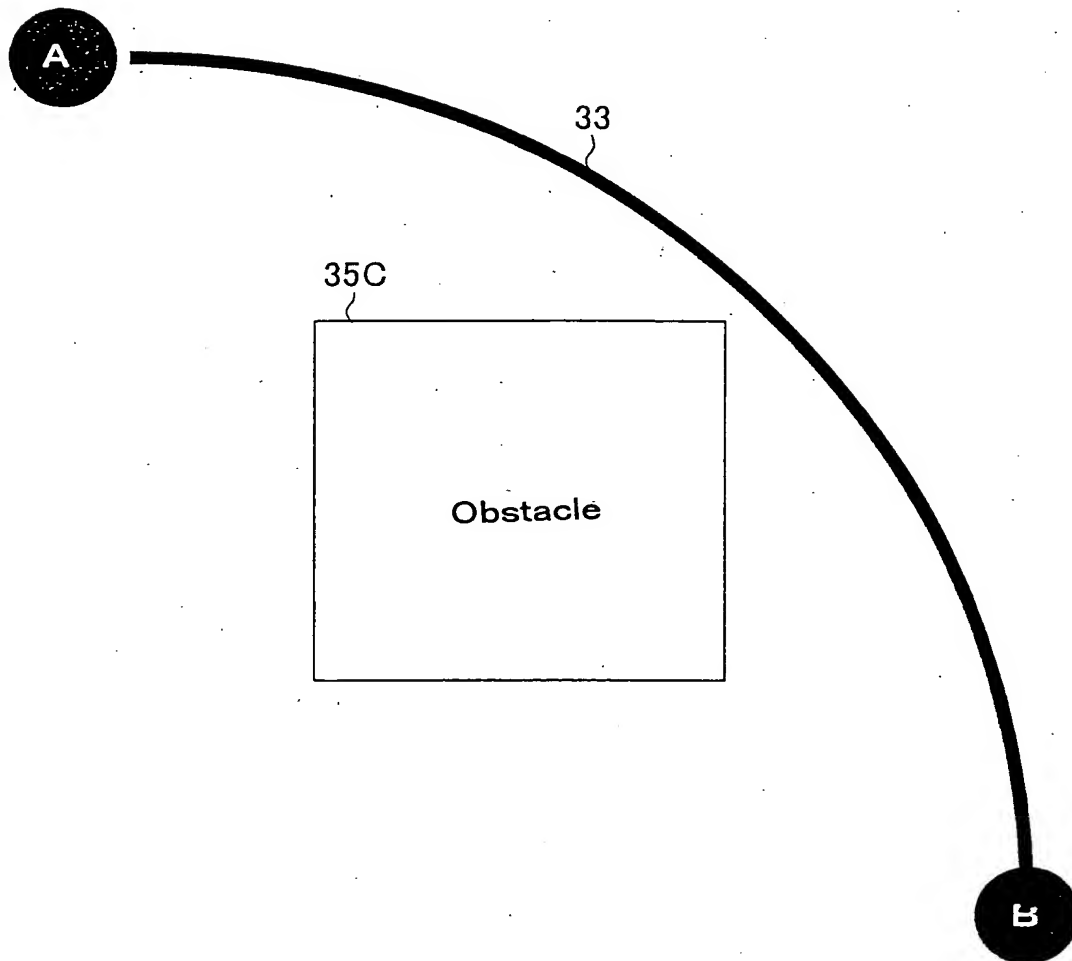




FIG. 39



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FIG. 40

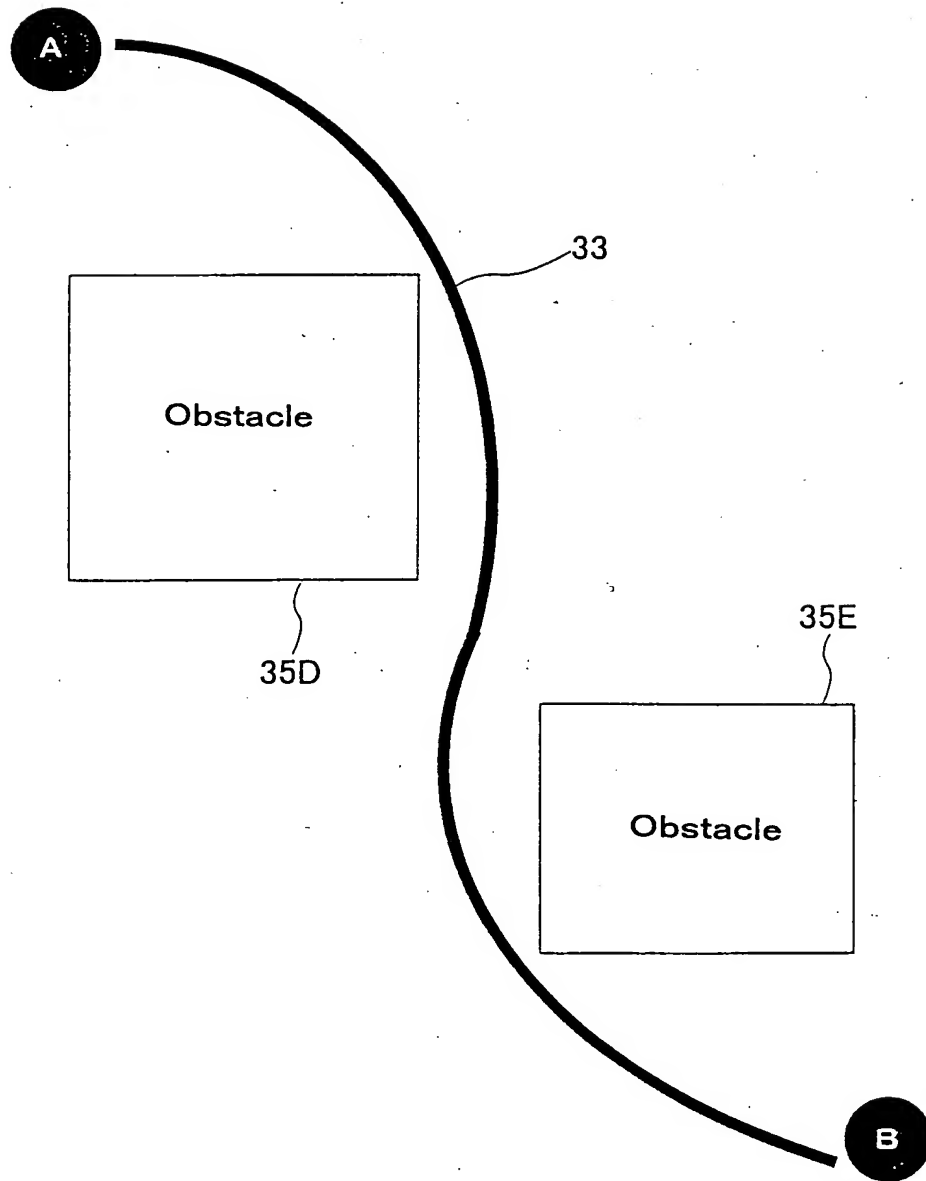


FIG. 41

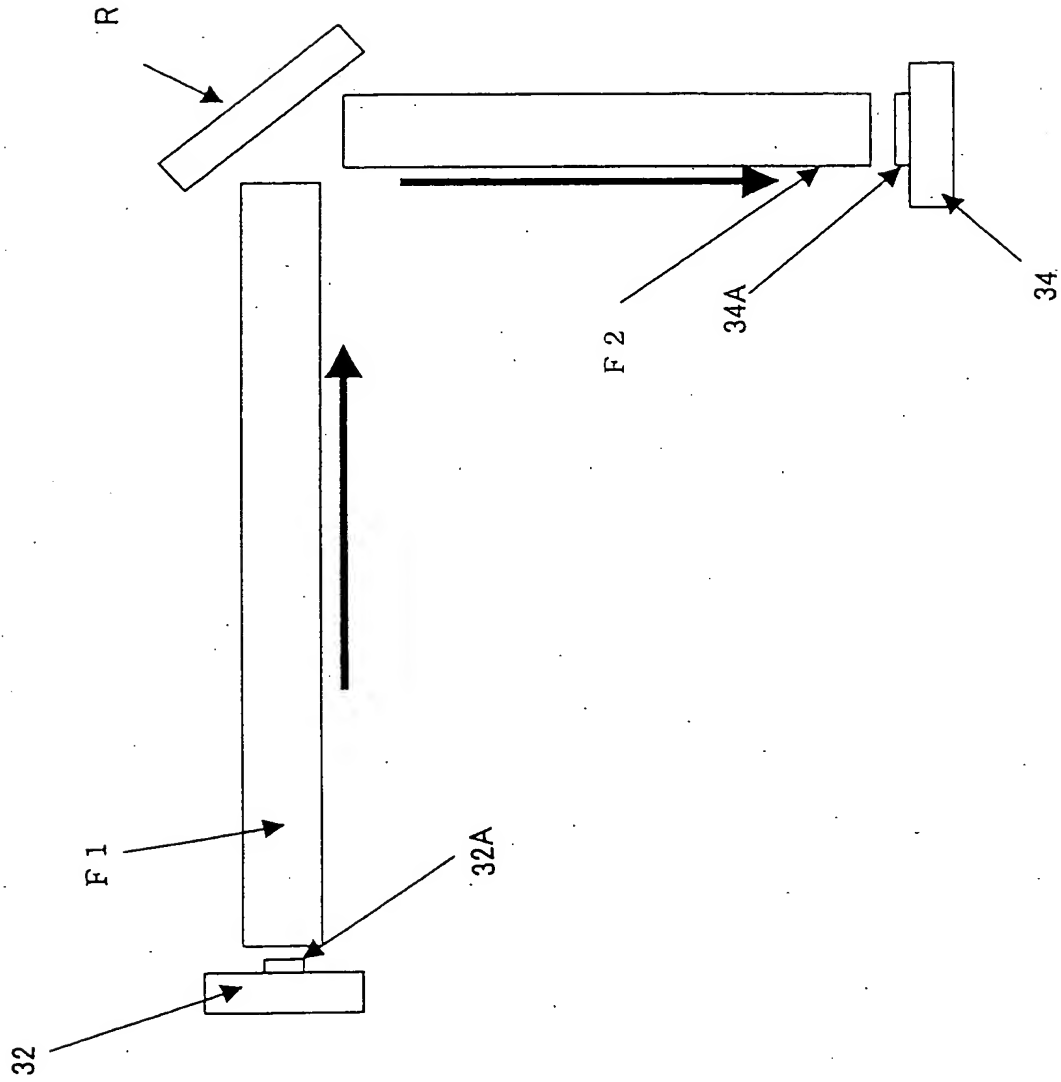


FIG. 42

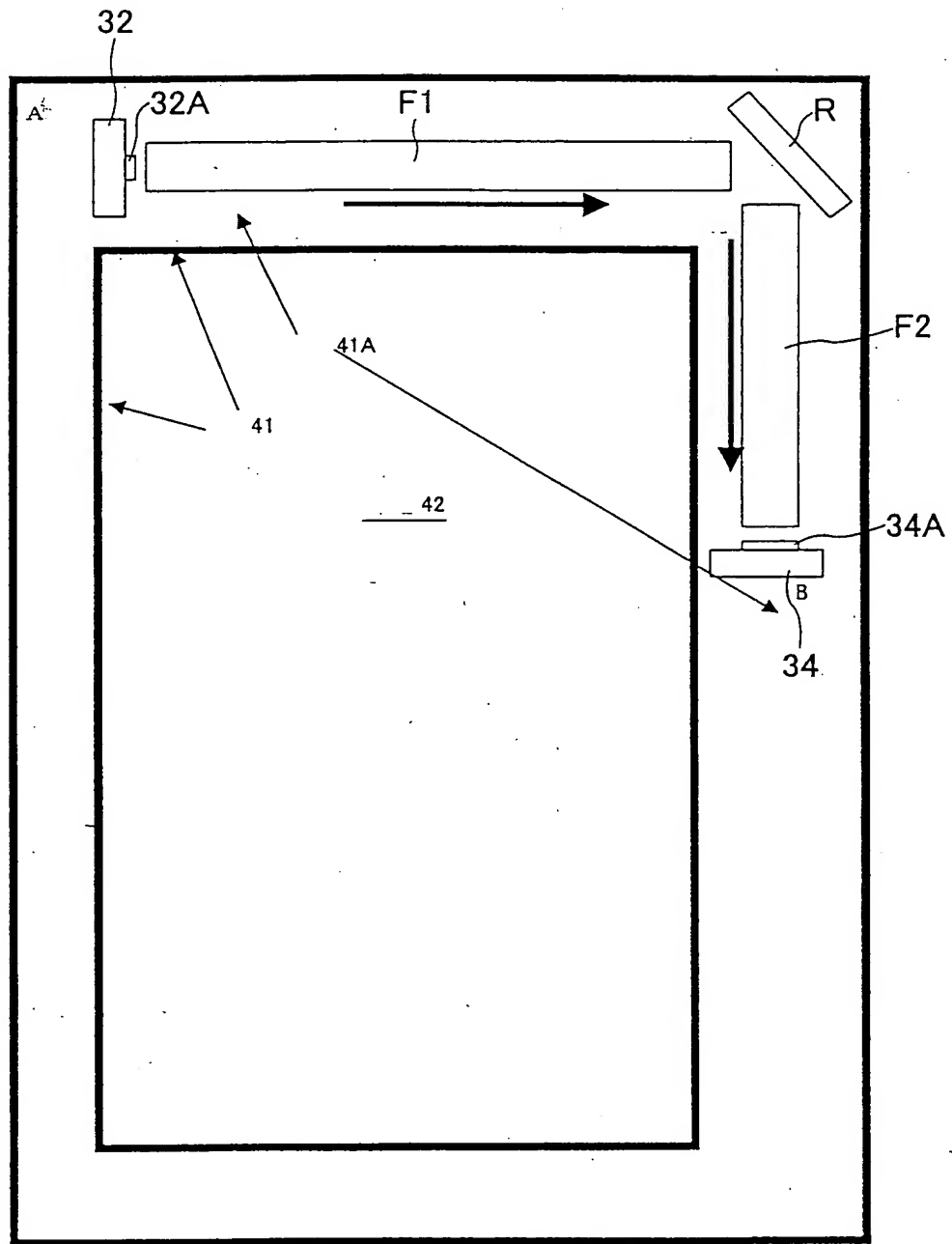


FIG. 43

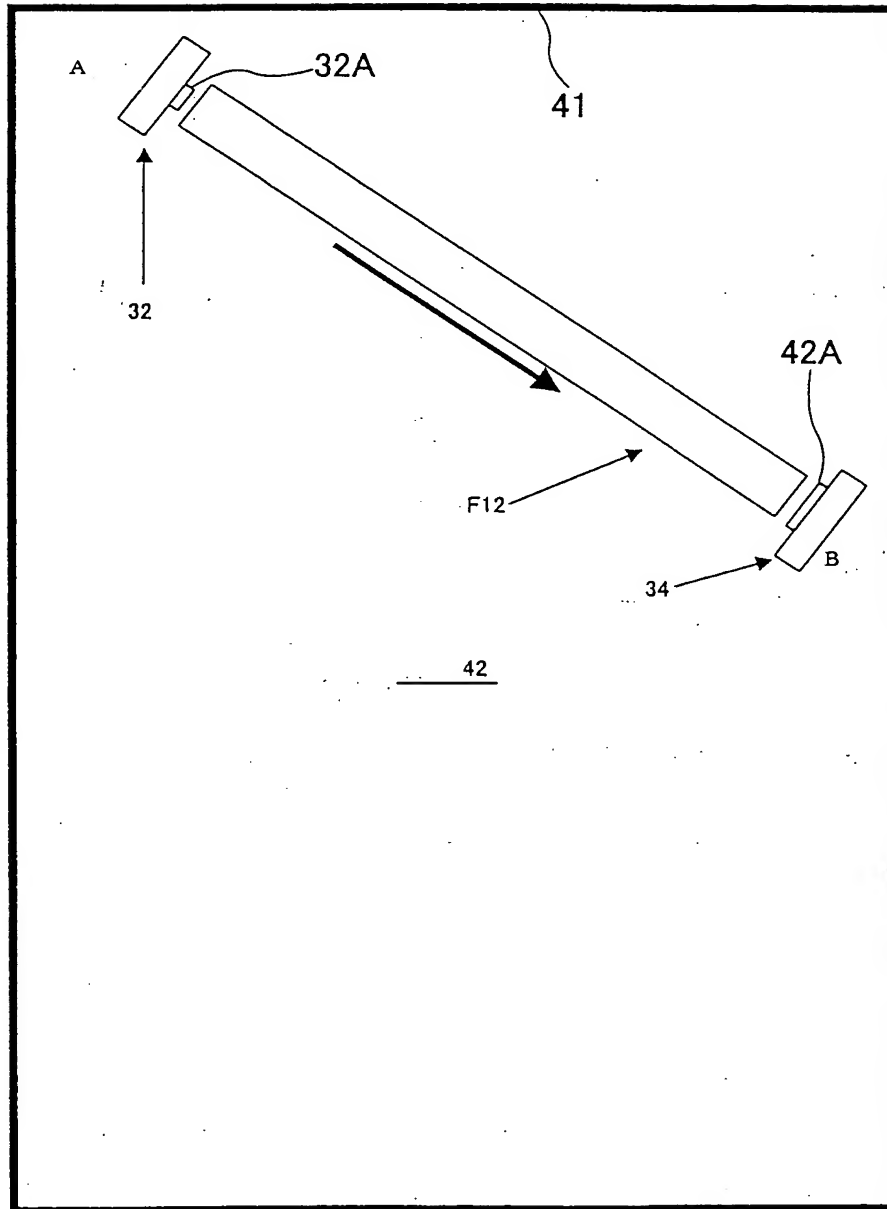


FIG. 44

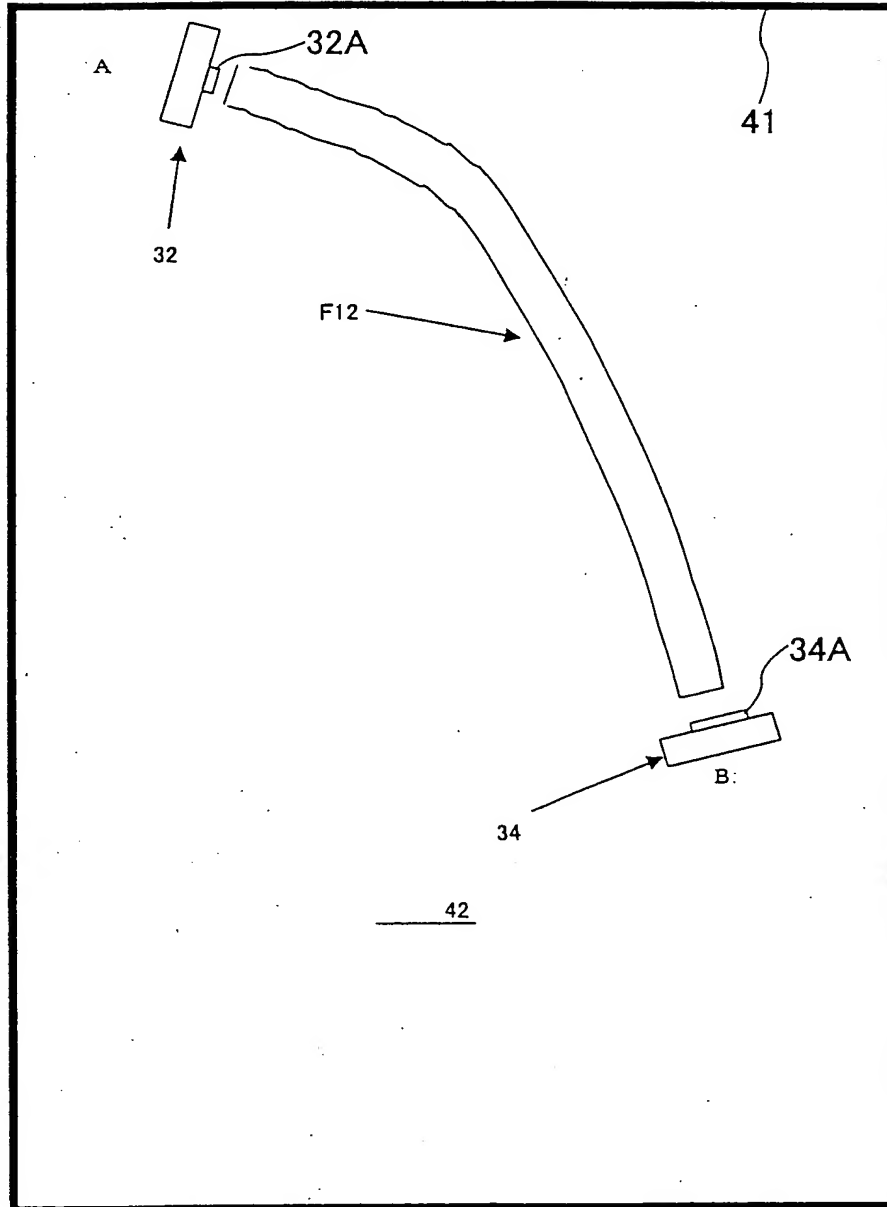


FIG. 45

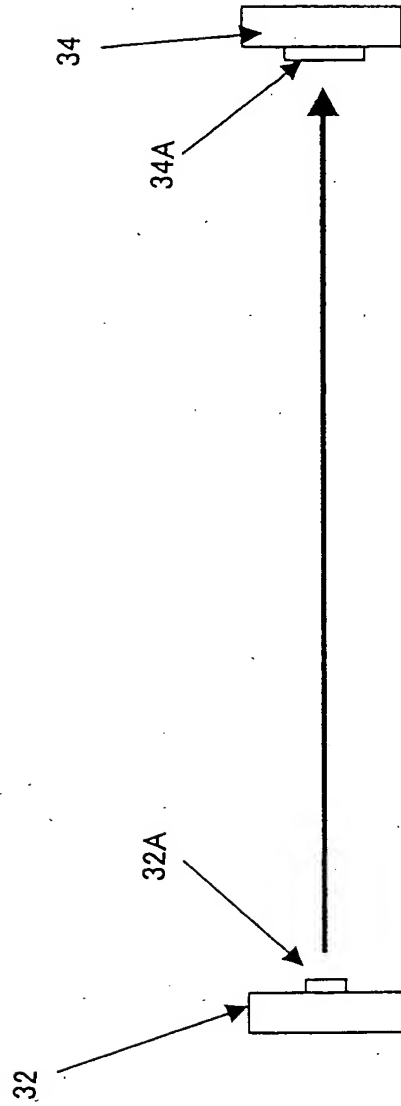


FIG. 46

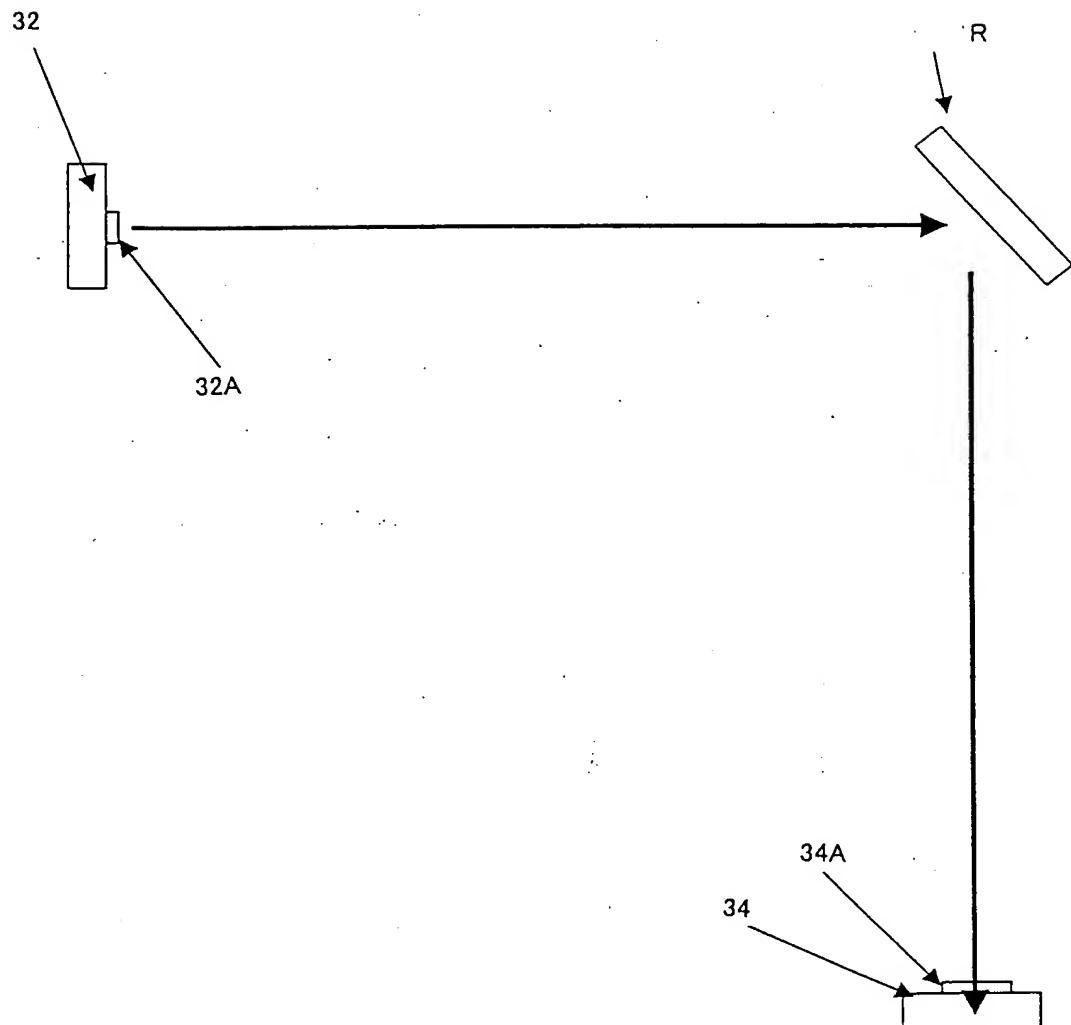
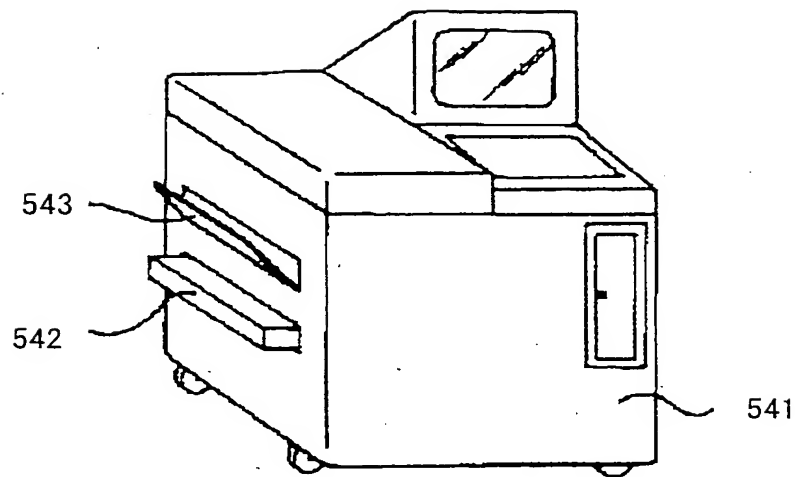




FIG. 47



[illegible]

FIG. 49

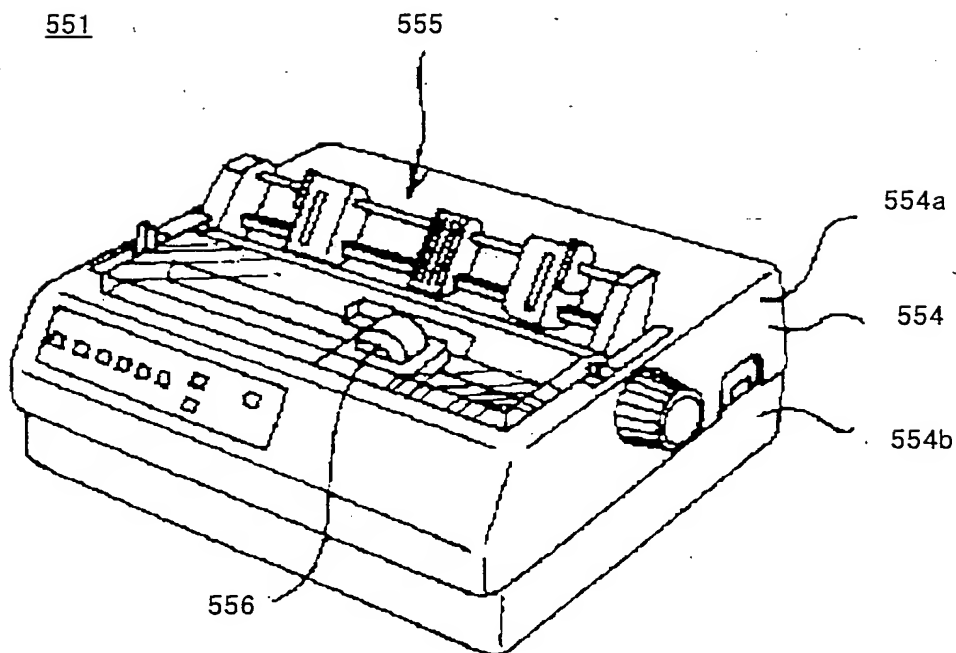


FIG. 50

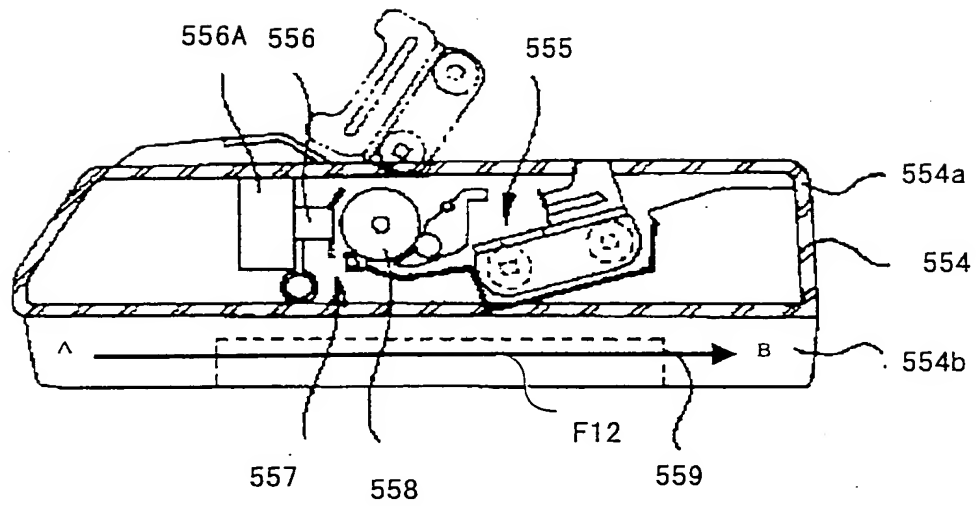


FIG. 51

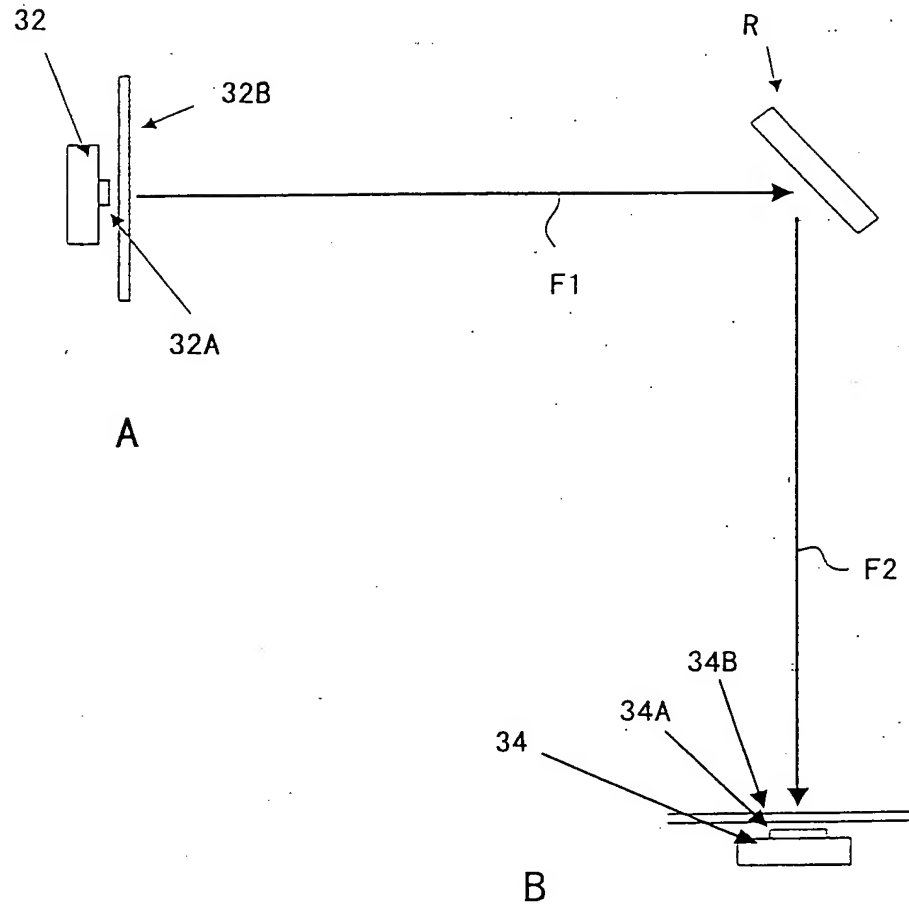


FIG. 52

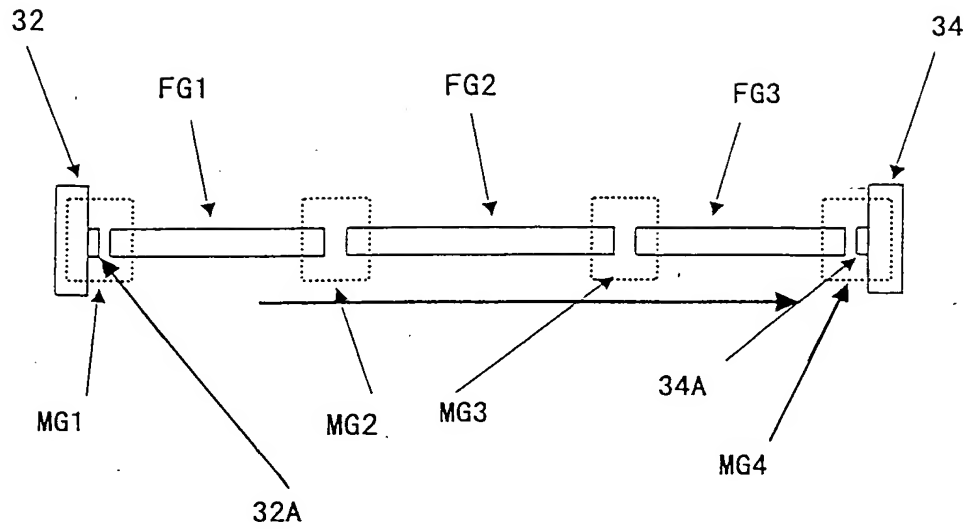


FIG. 53

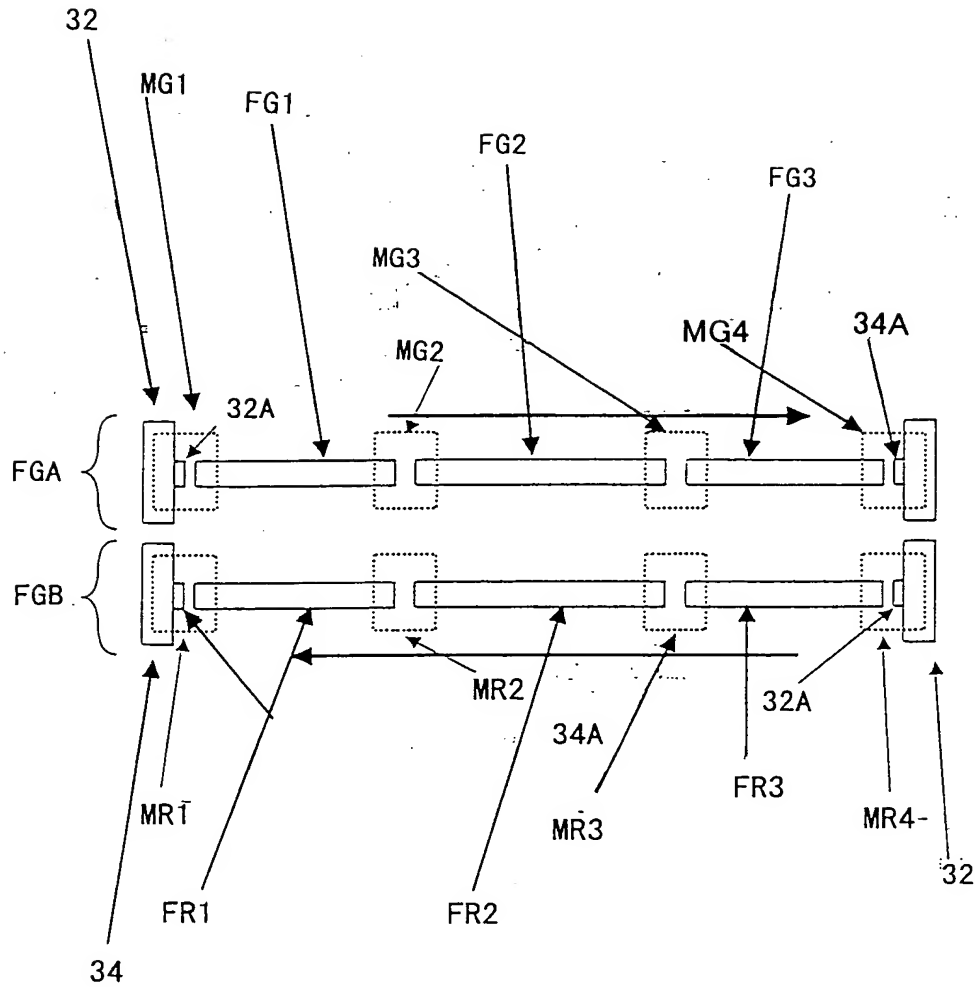


FIG. 54

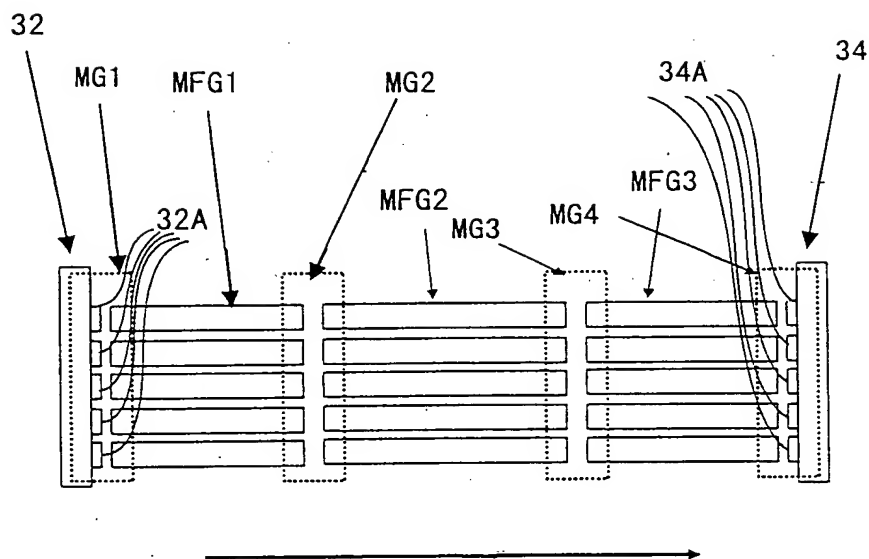




FIG. 55

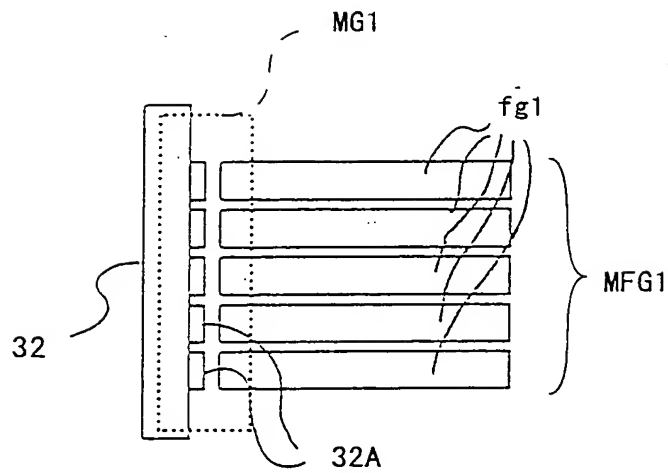


FIG. 56

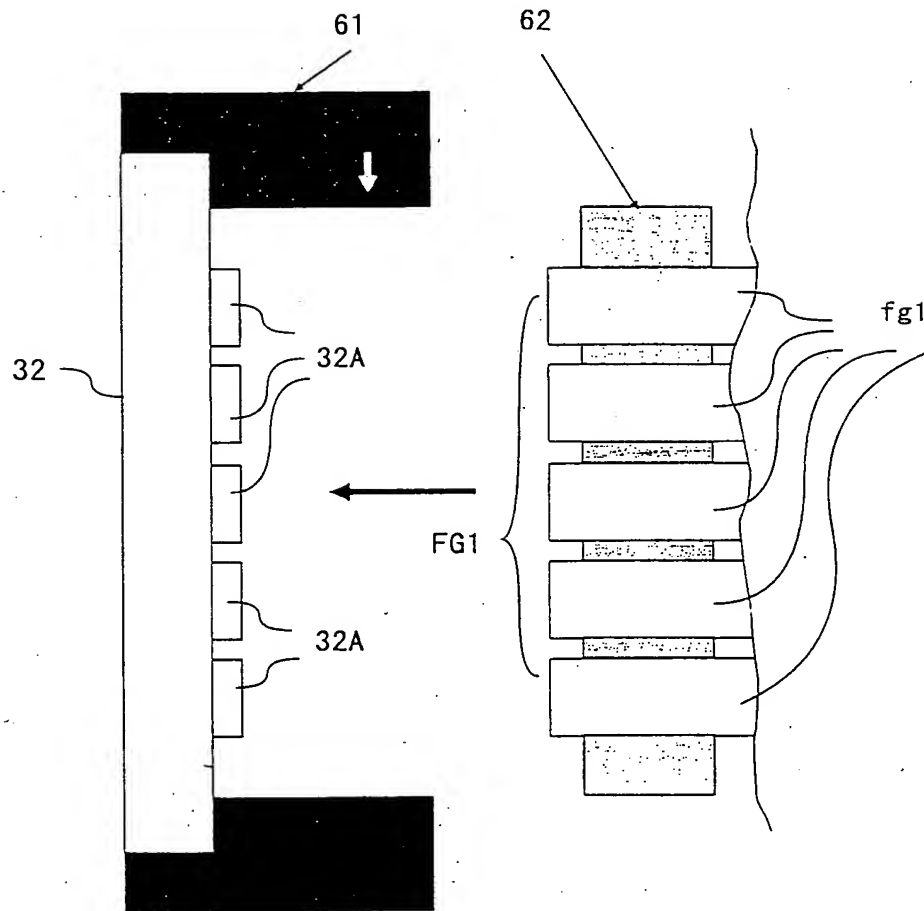


FIG. 57

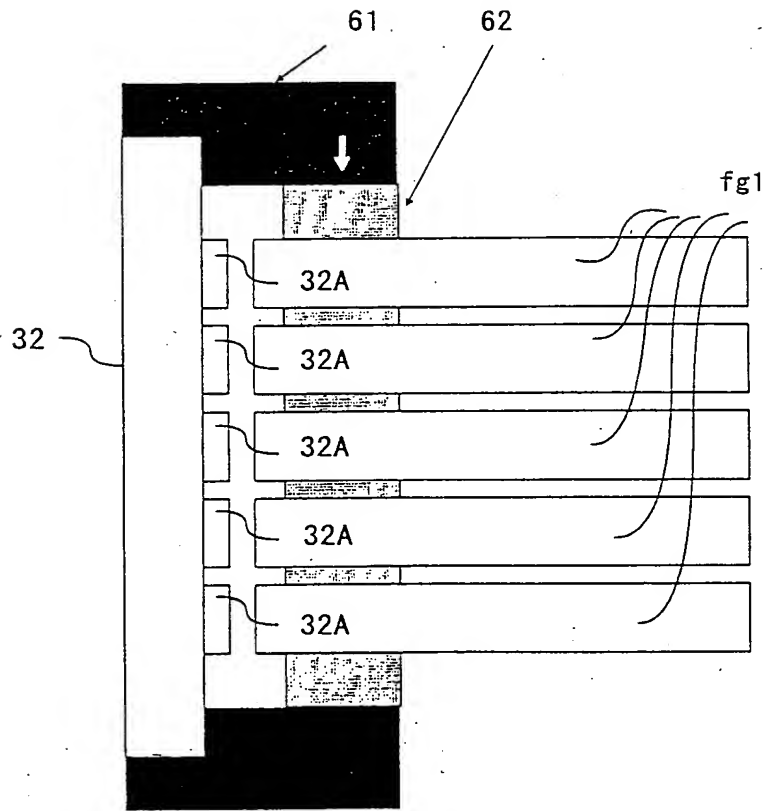
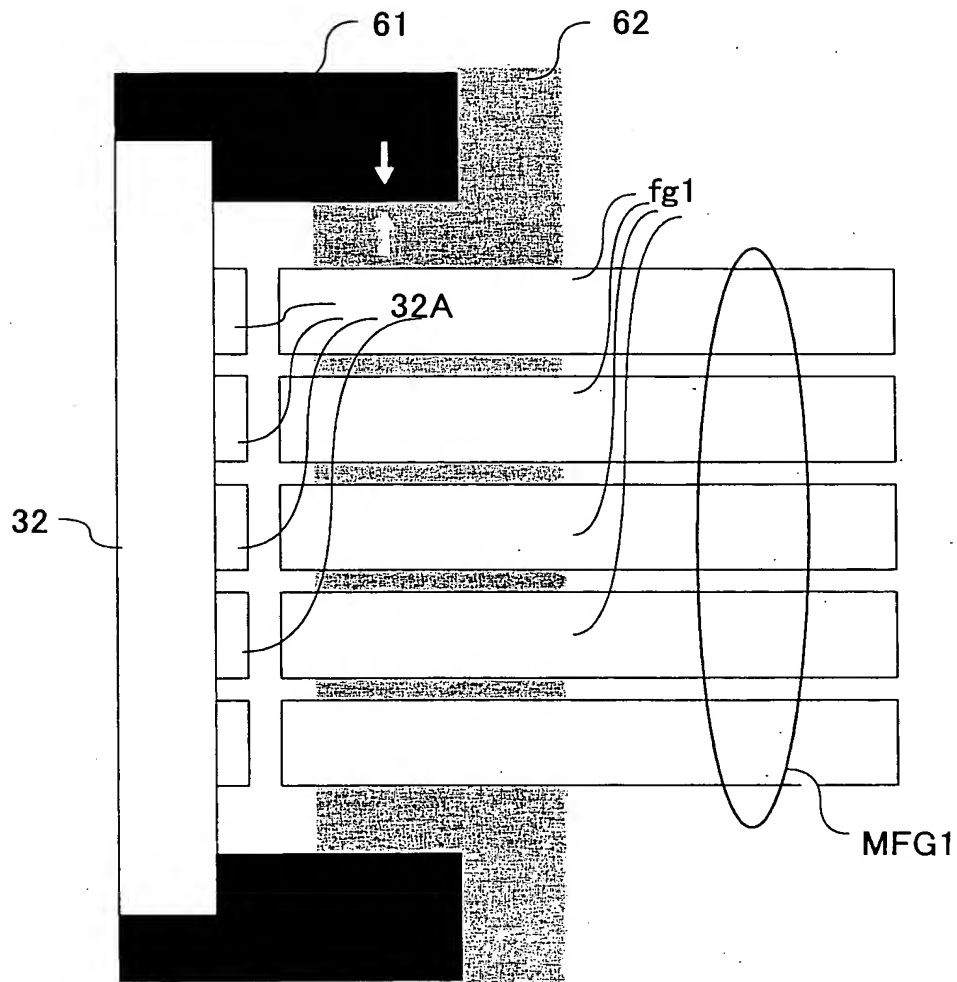




FIG.59



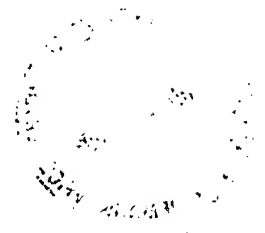


FIG.61

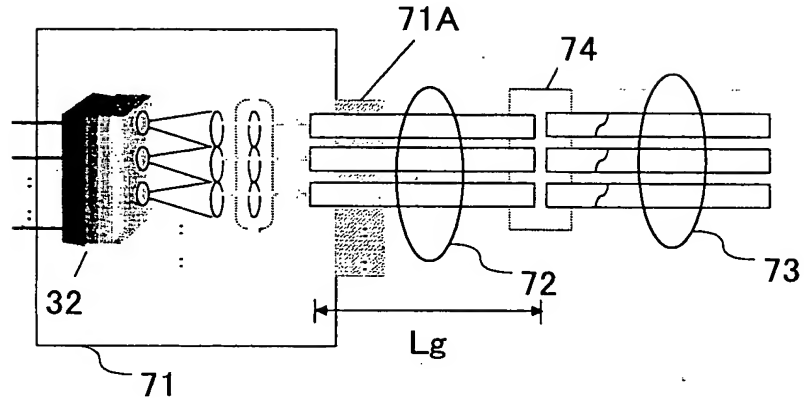


FIG.62

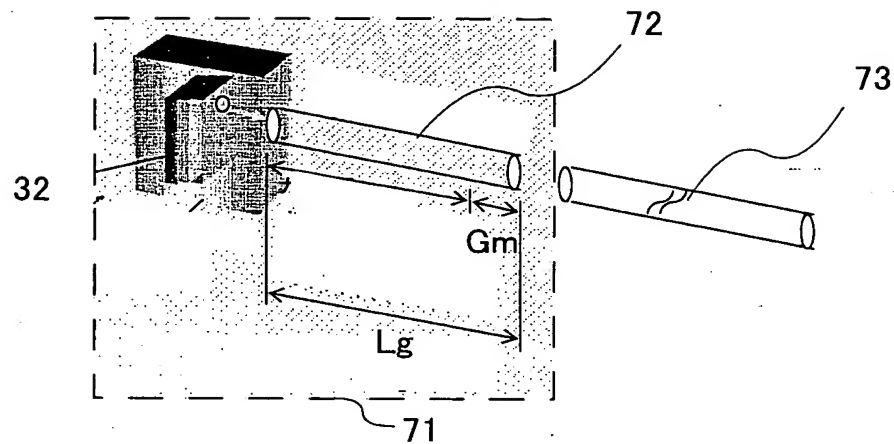




FIG.63

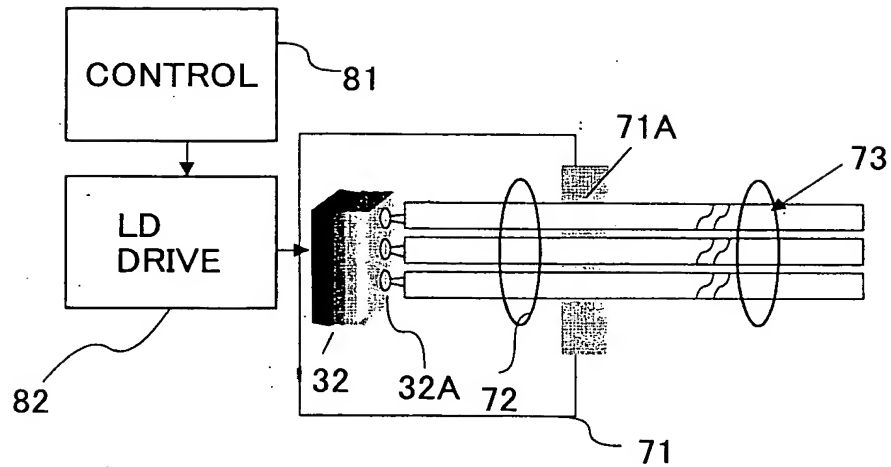


FIG. 64

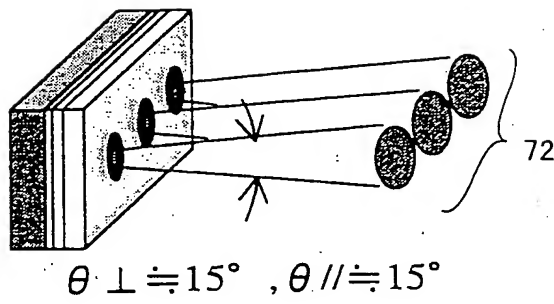


FIG. 65A

FIG. 65C

FIG. 65B

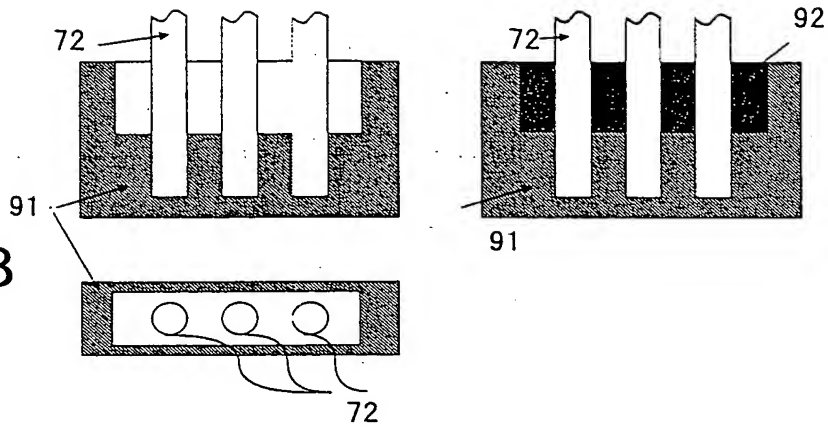


FIG. 66A

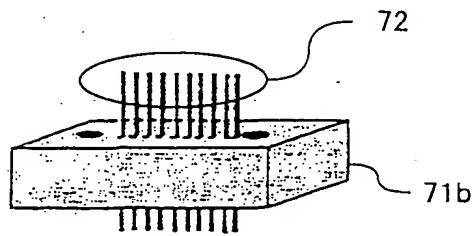


FIG. 66B

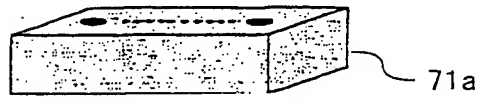


FIG. 66C

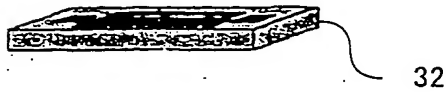
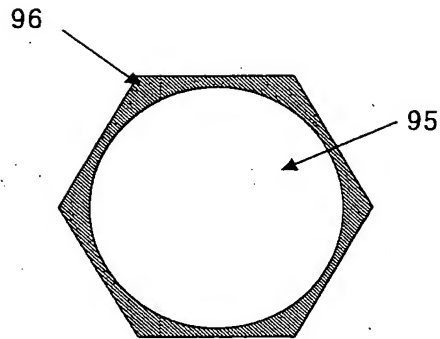


FIG. 67



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FIG. 68

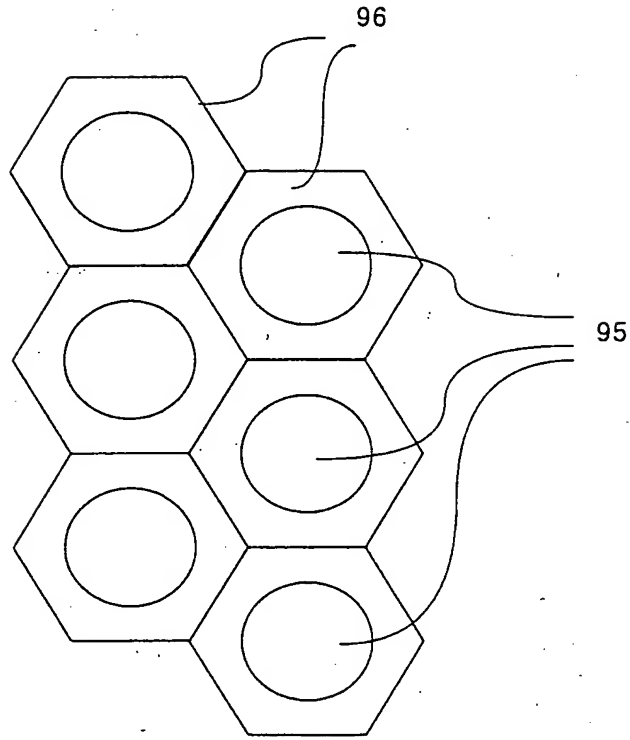


FIG. 69

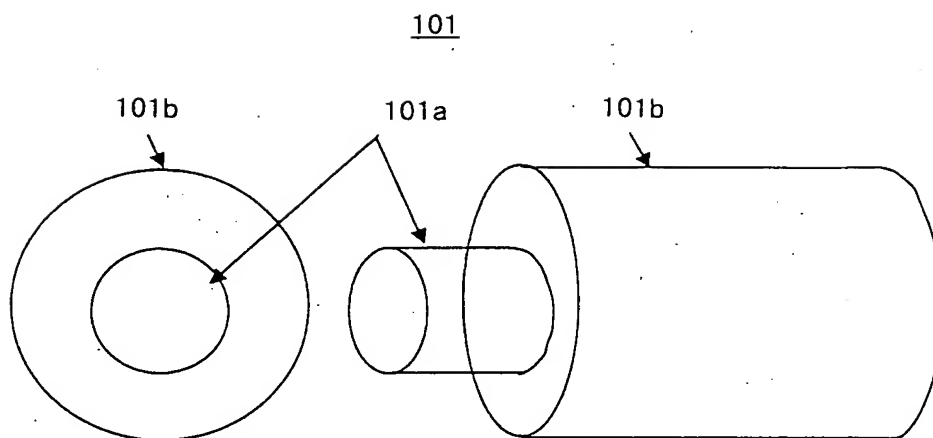


FIG. 70

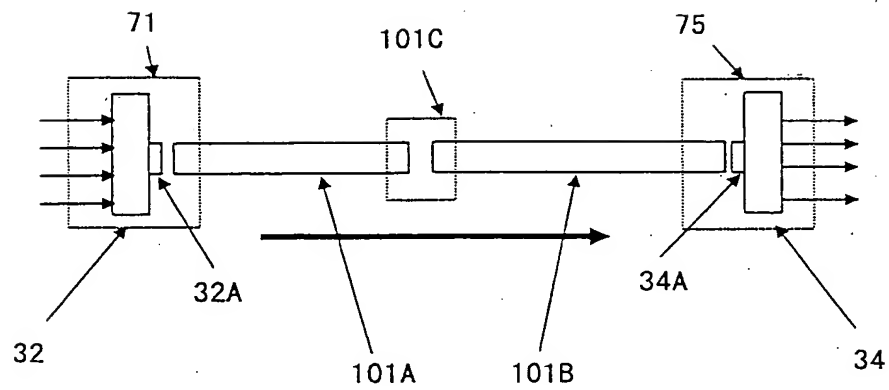




FIG. 71

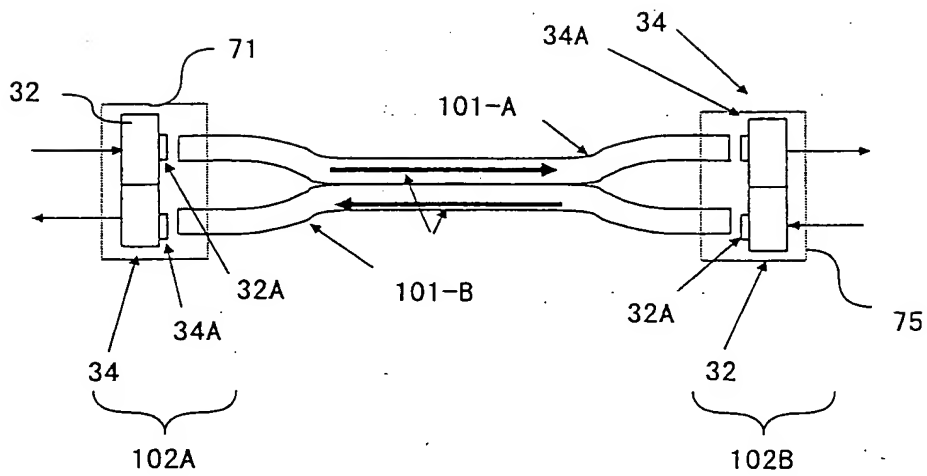


FIG. 72

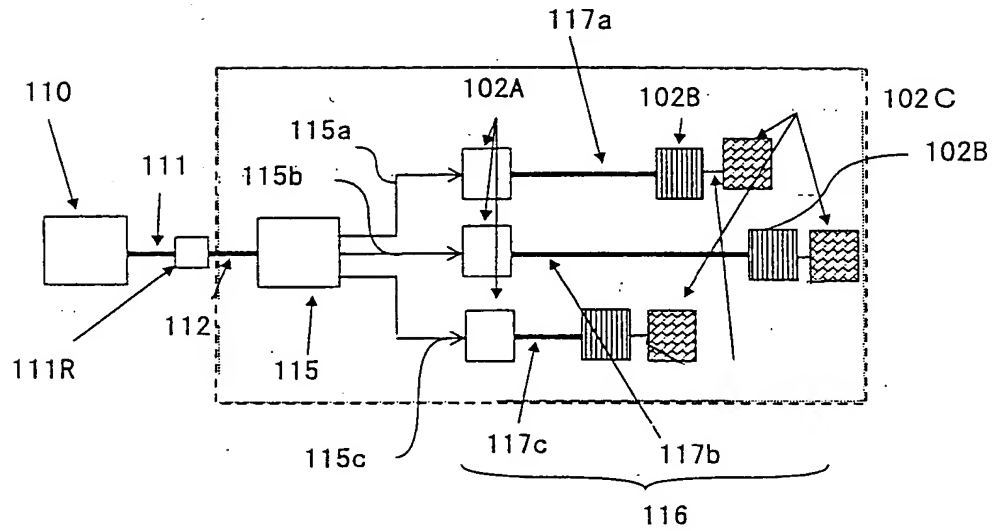


FIG. 73A

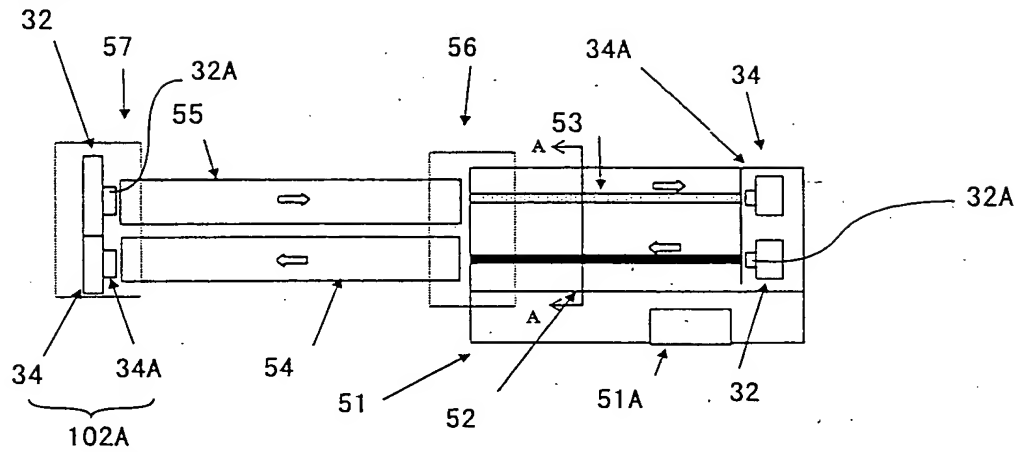


FIG. 73B

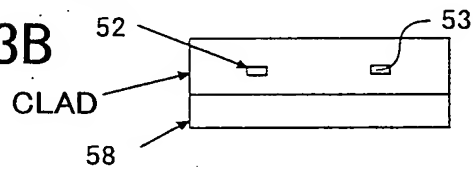


FIG. 74A

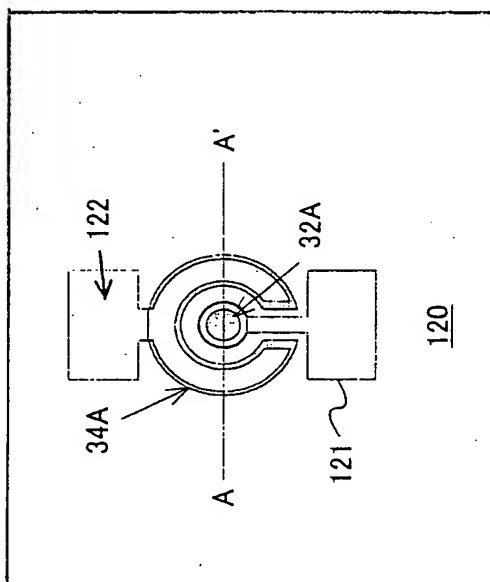


FIG. 74B

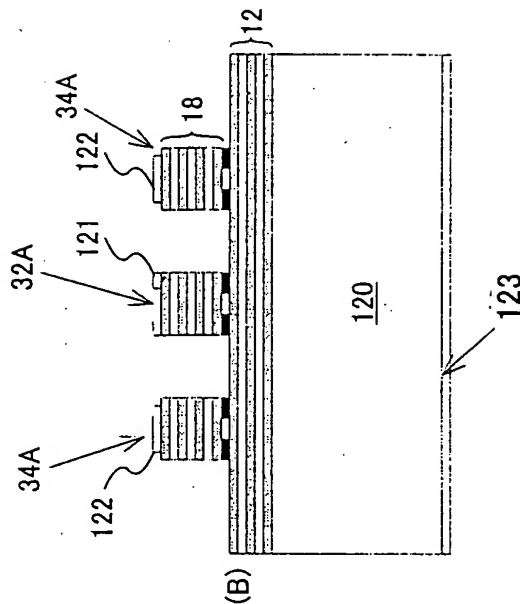


FIG. 75

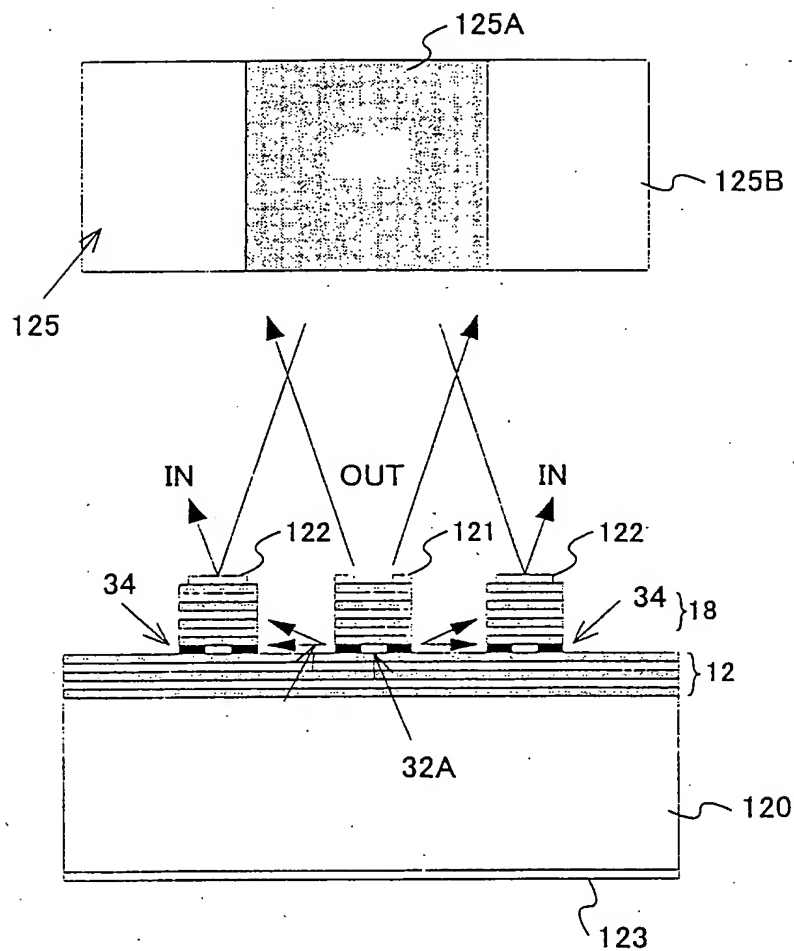


FIG. 76A

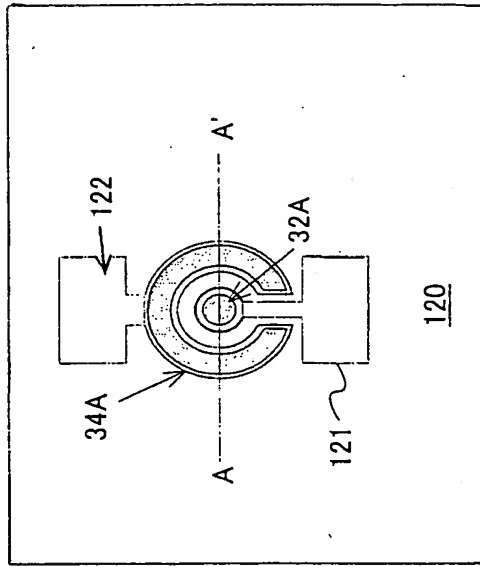


FIG. 76B

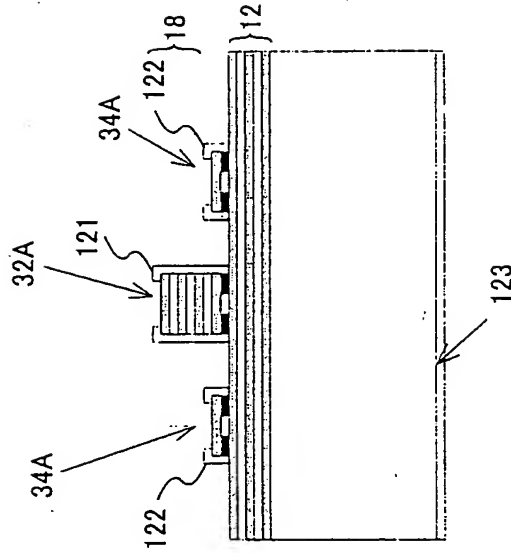


FIG. 77

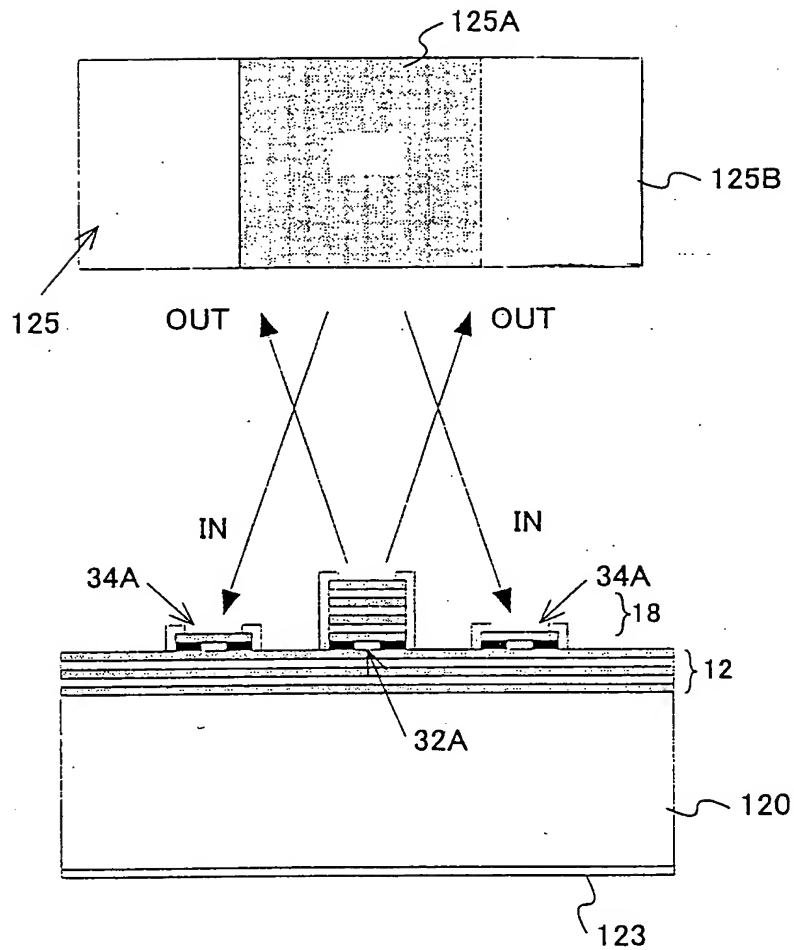


FIG. 78

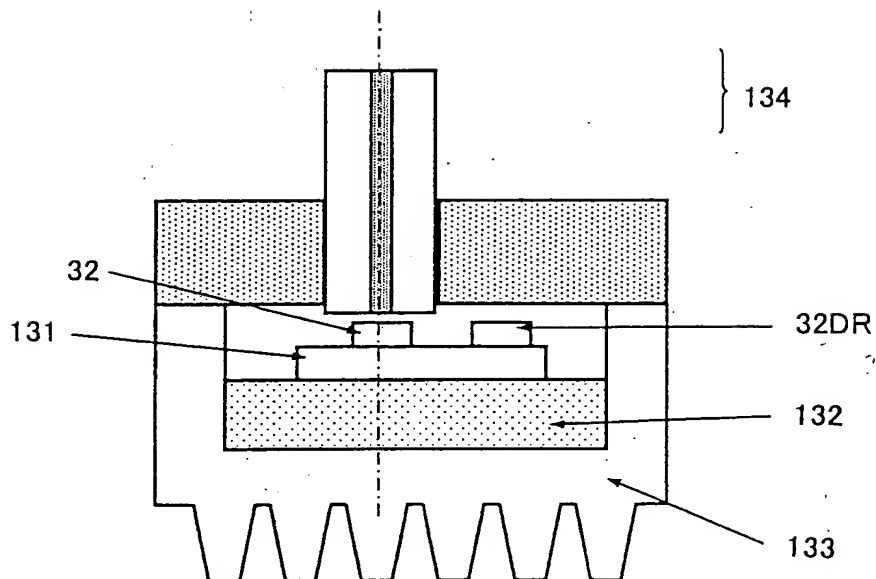
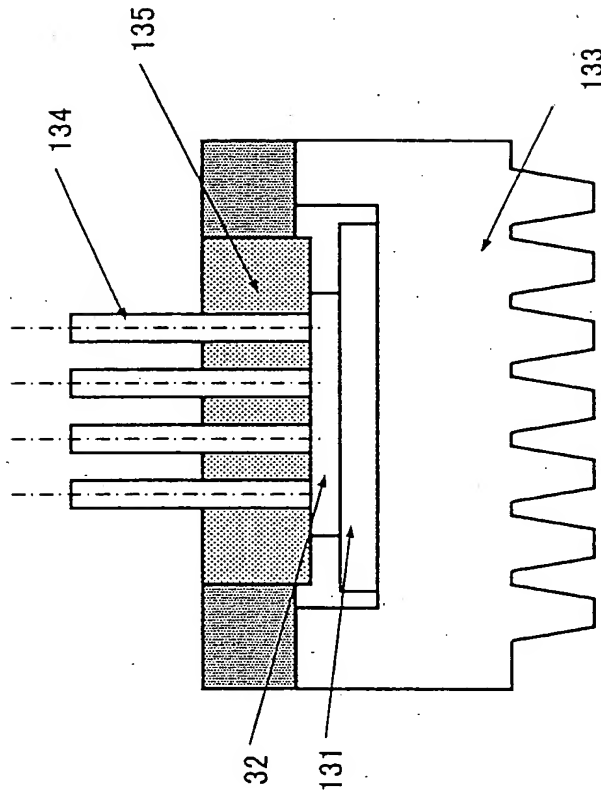




FIG. 79



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FIG. 80

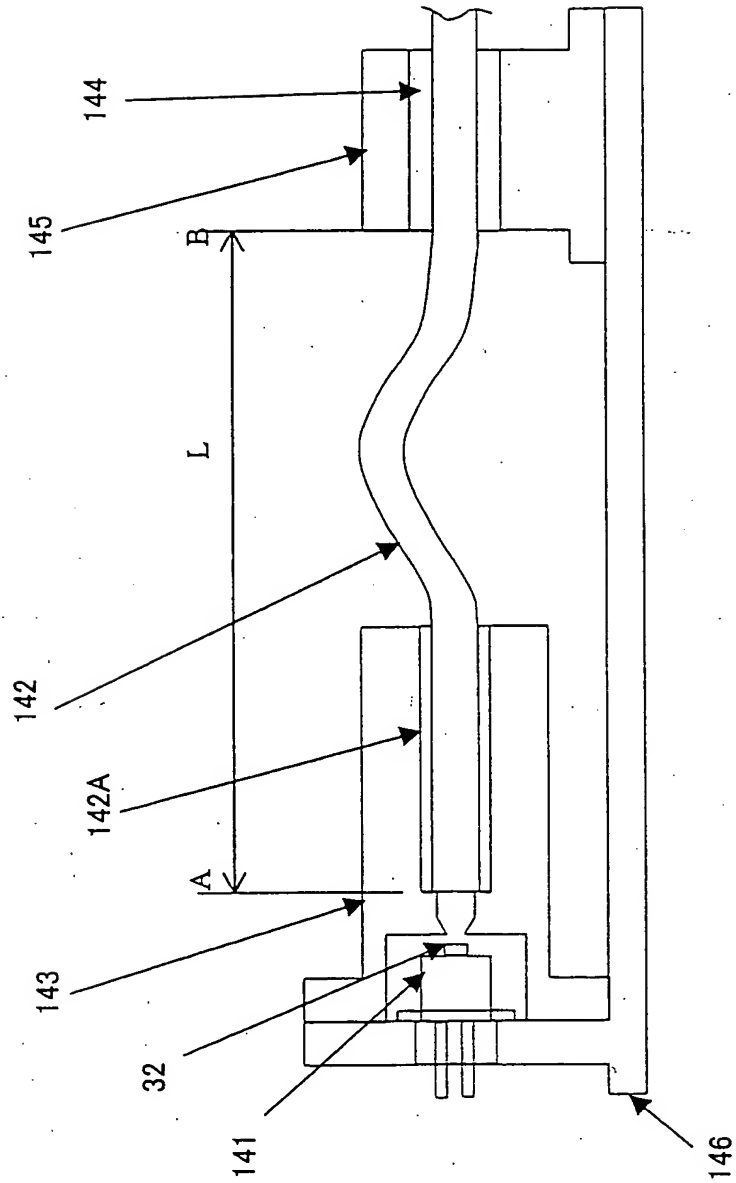


FIG. 81

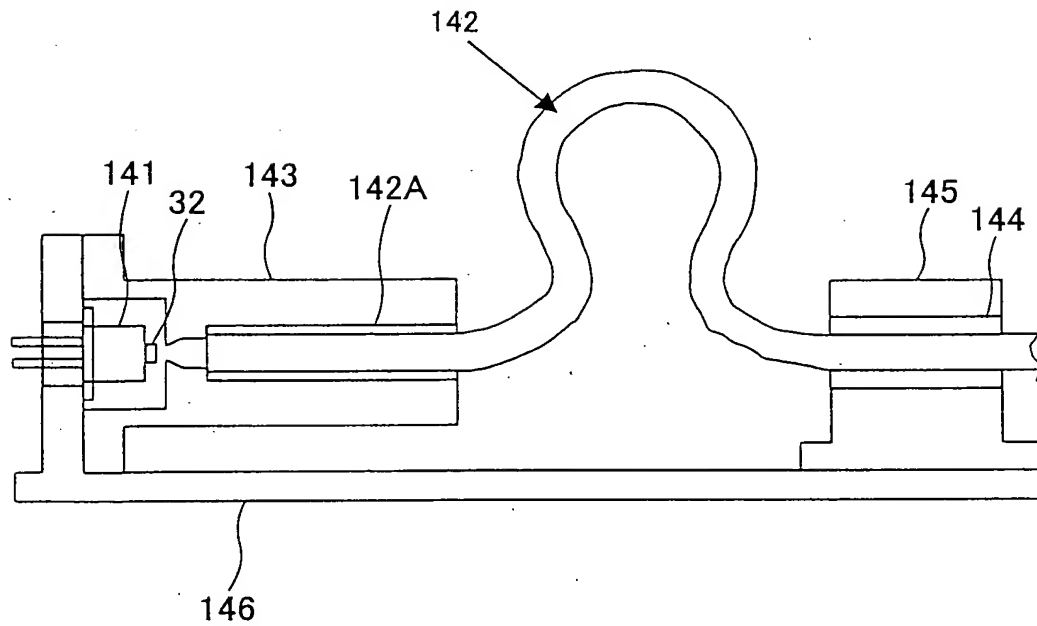
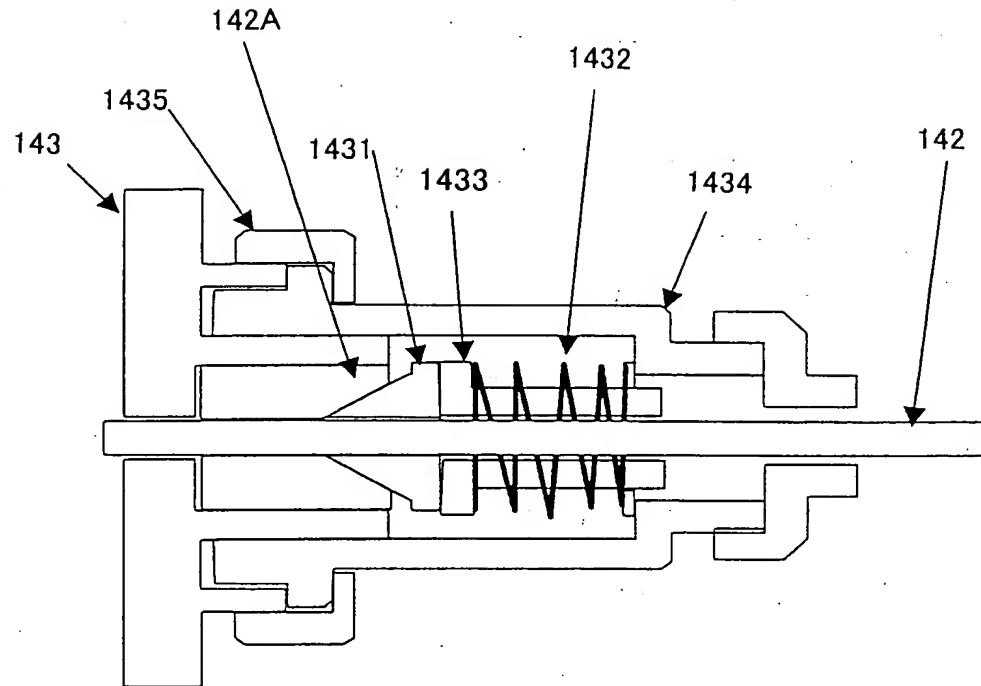


FIG. 82



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FIG. 83

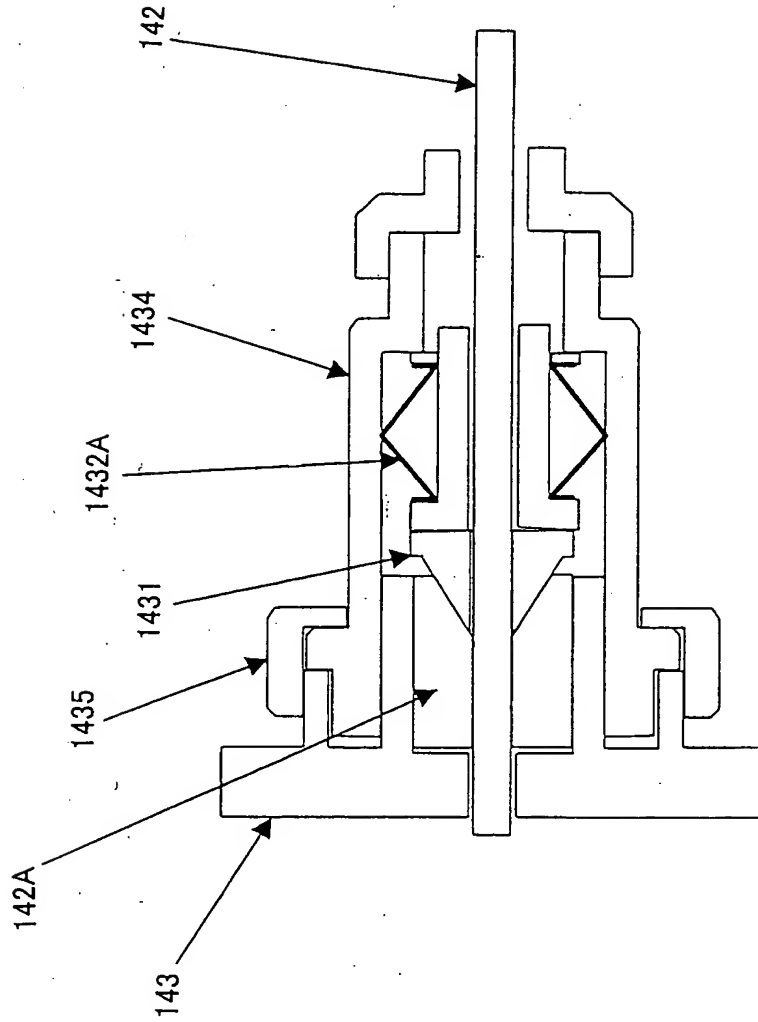


FIG. 84

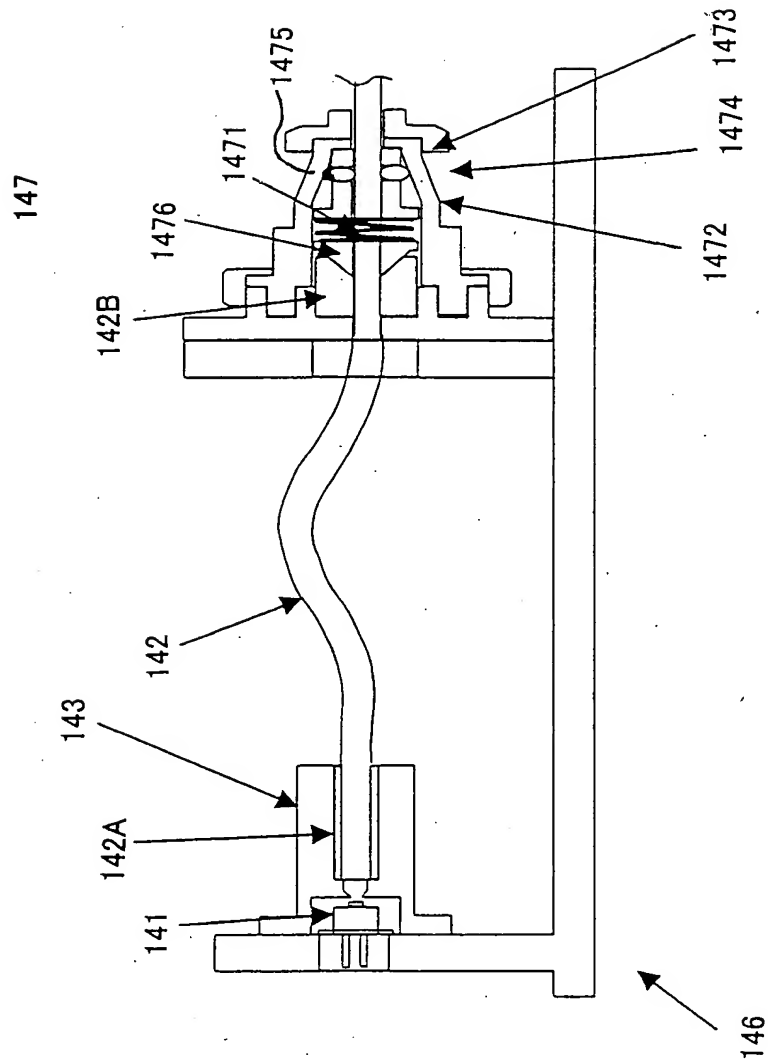
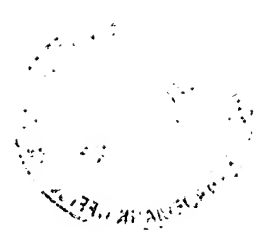
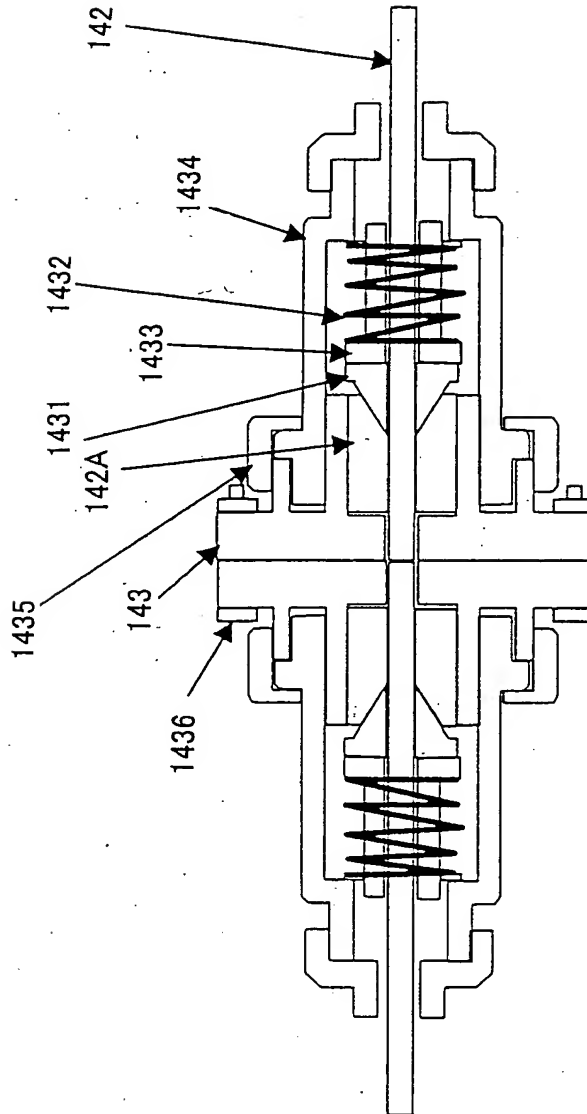


FIG. 85



This diagram shows a cross-sectional view of a semiconductor device. It features a grid of vertical pillars (142) and horizontal lines (142P) on a substrate (131). The pillars are arranged in a regular pattern. A label 151 points to one of the pillars, and 151A points to a specific feature on its top surface. A label 32 points to a small rectangular feature on the horizontal lines. The substrate is labeled 131.





FIG. 87

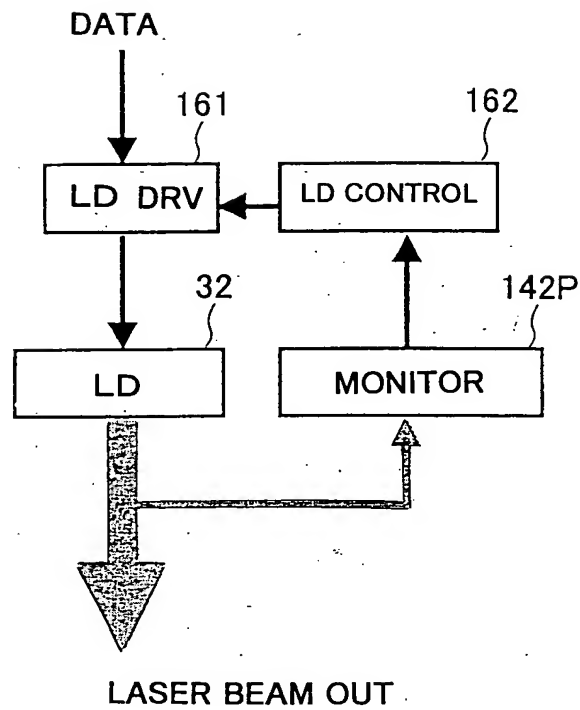


FIG. 88

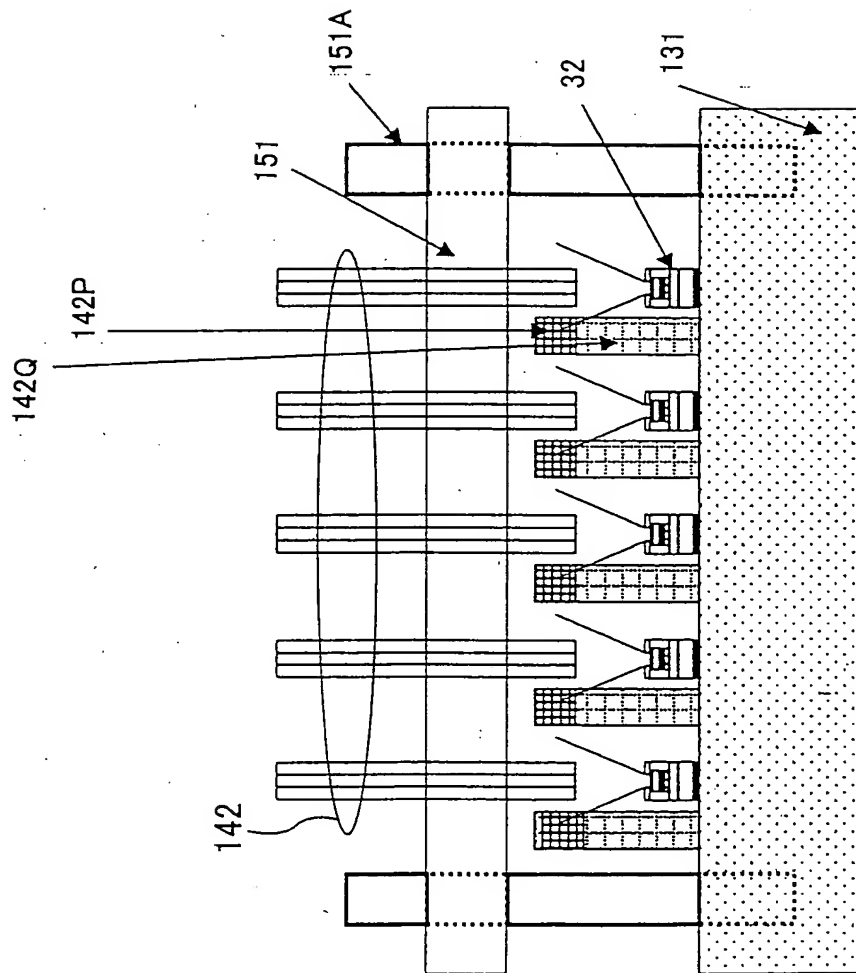


FIG. 89

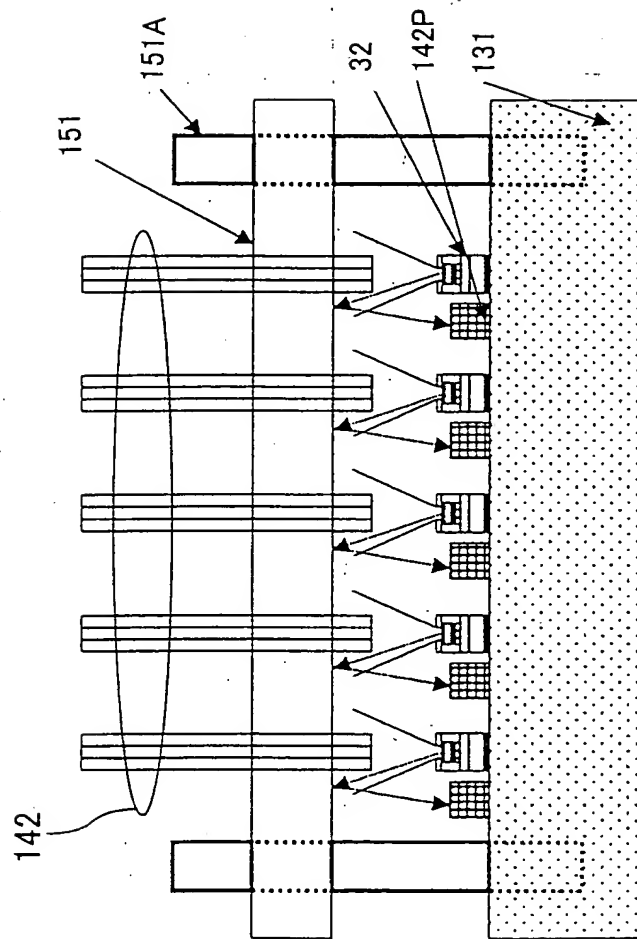
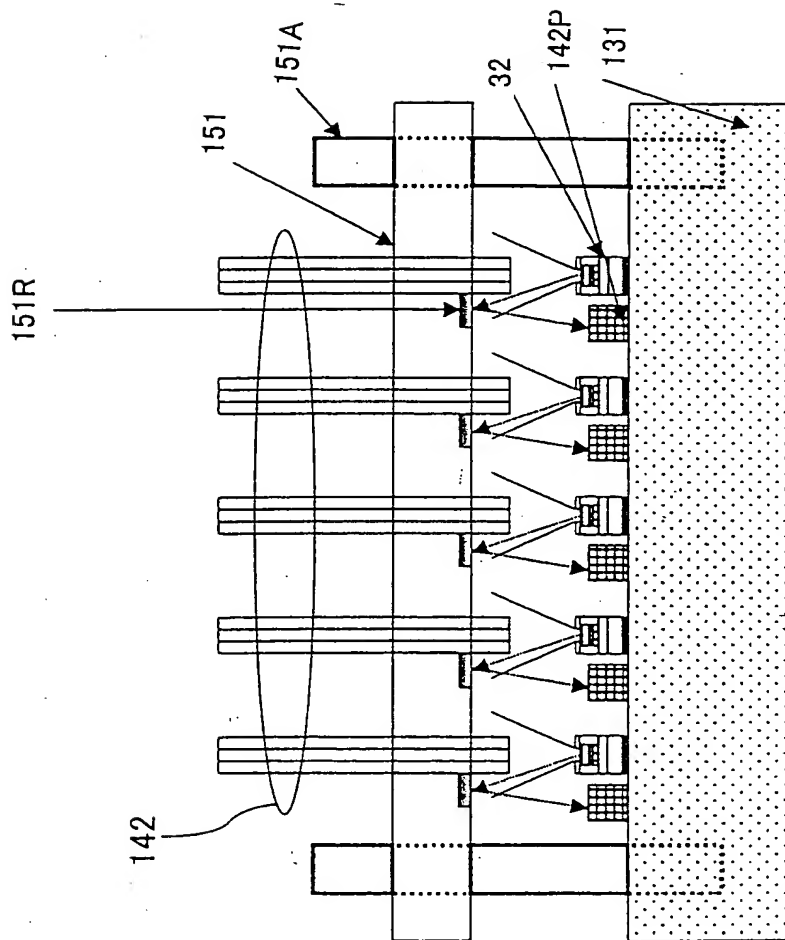


FIG. 90



**FIG. 91**

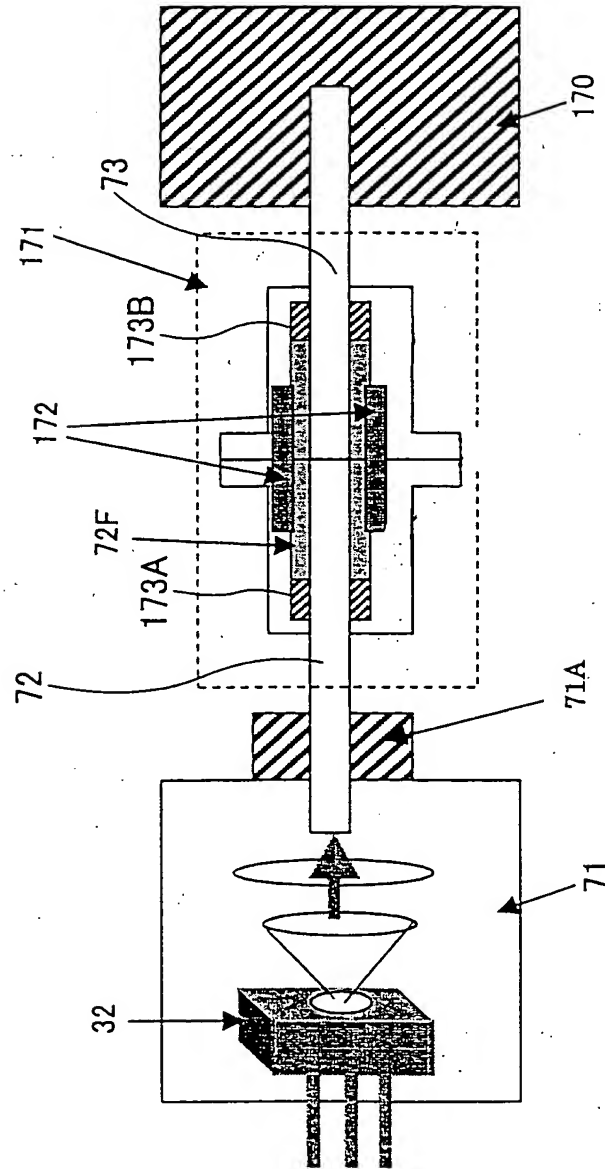


FIG. 92

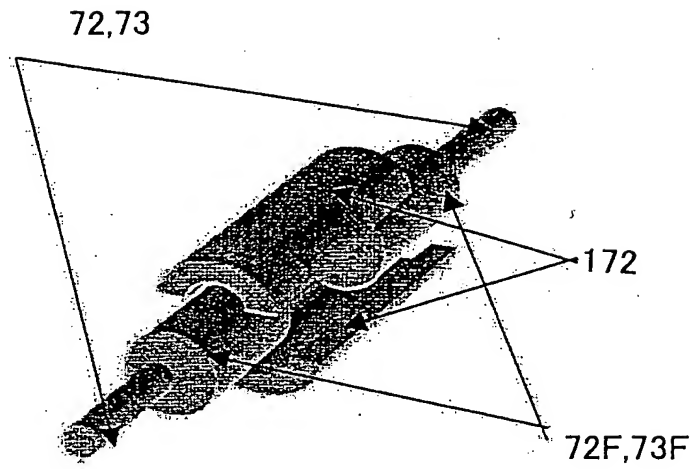


FIG. 93

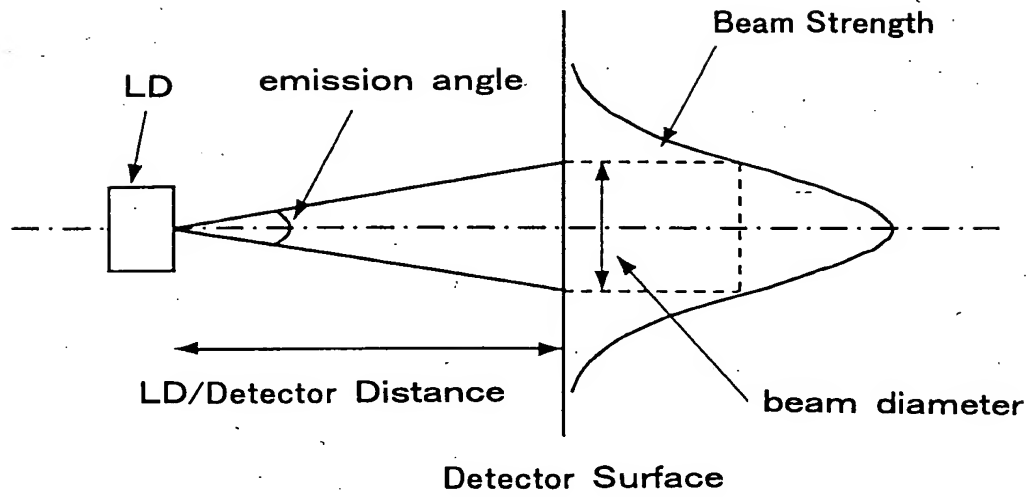


FIG. 94

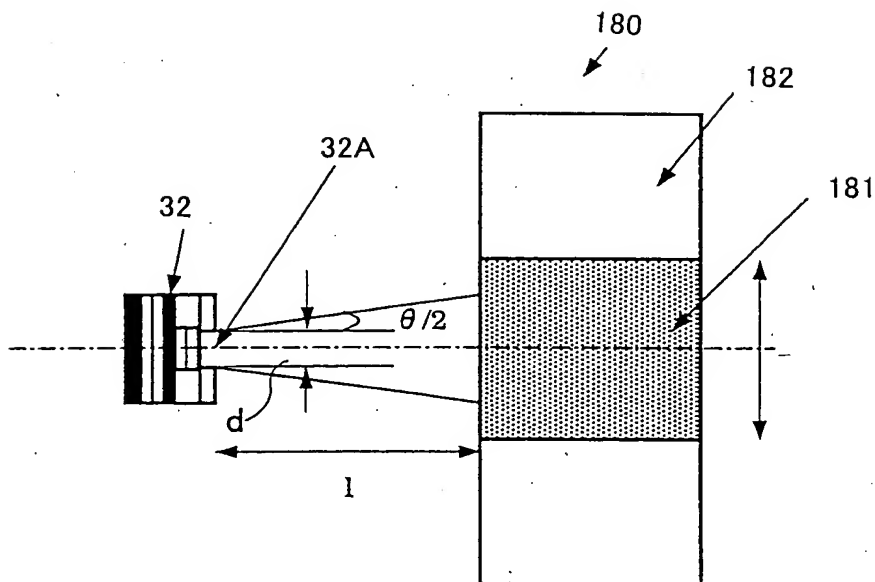




FIG.95

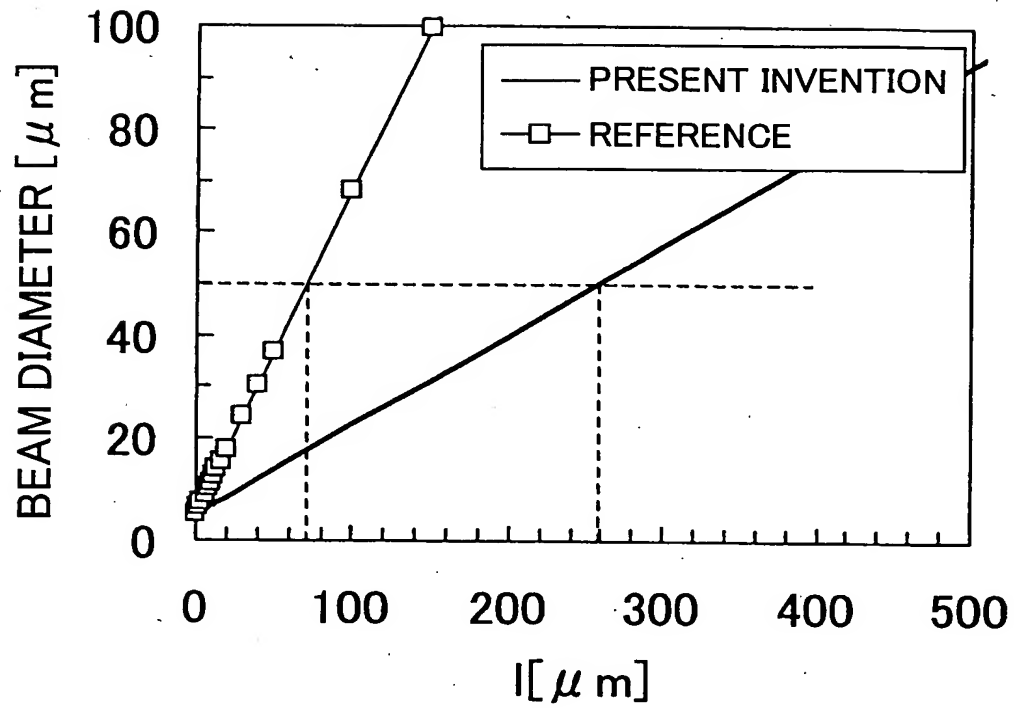
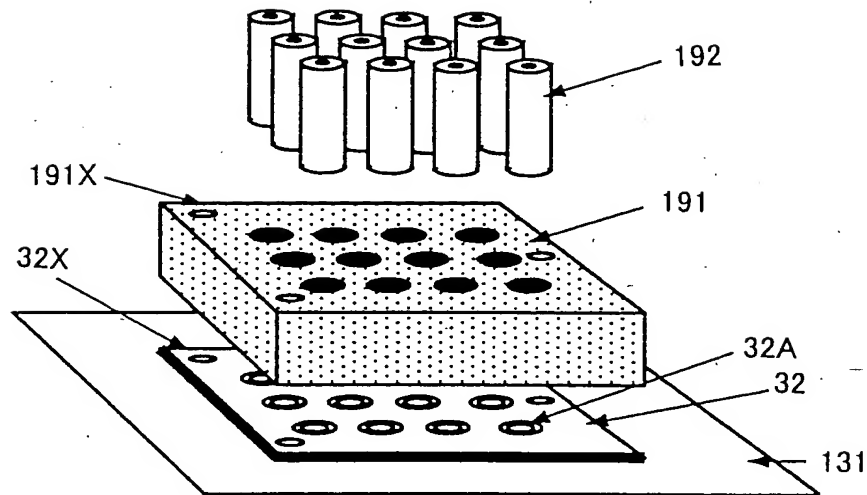


FIG. 96



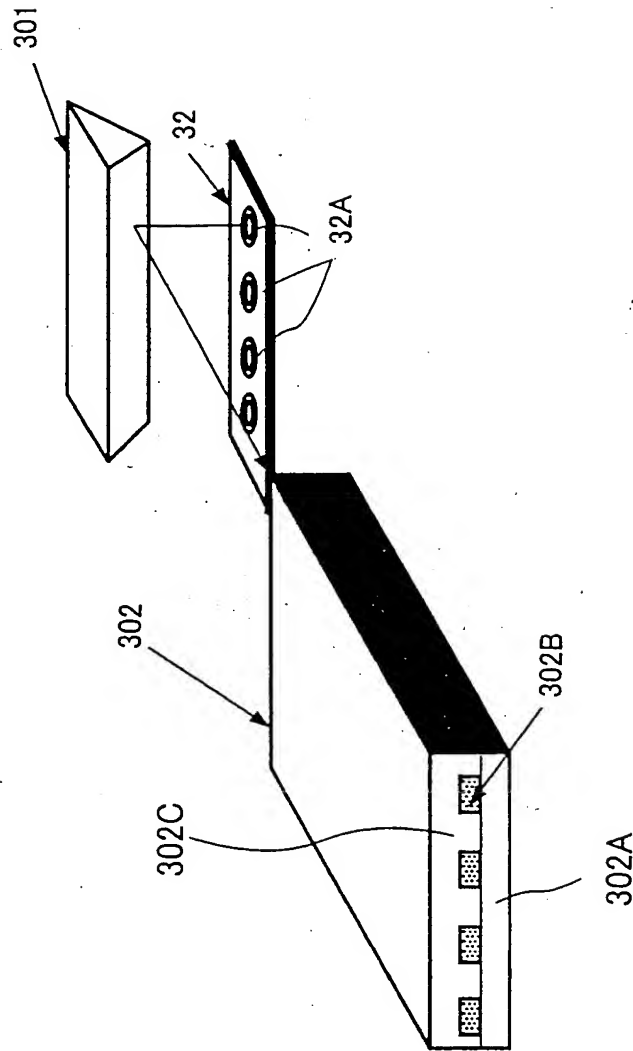


FIG. 97A

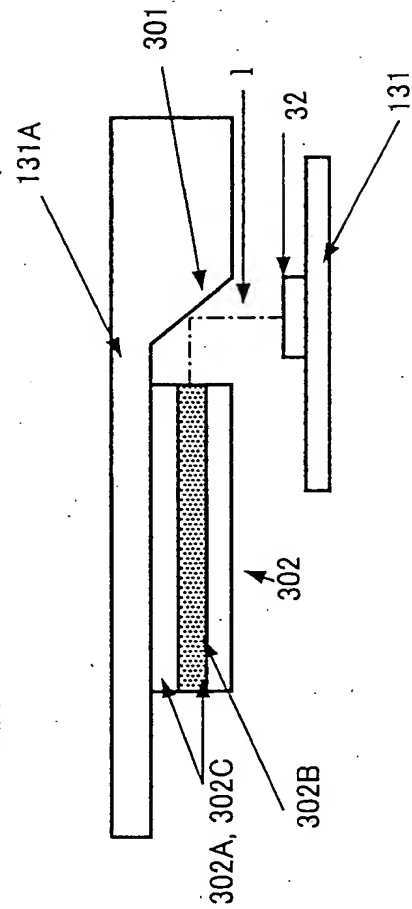
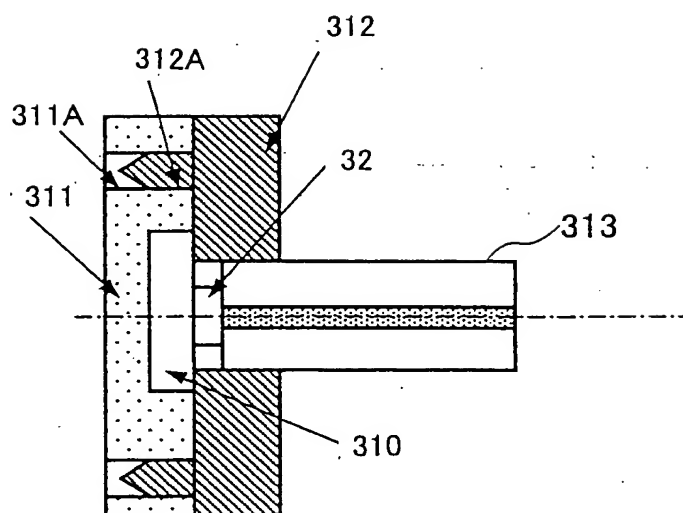


FIG. 97B

FIG. 98



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FIG. 99

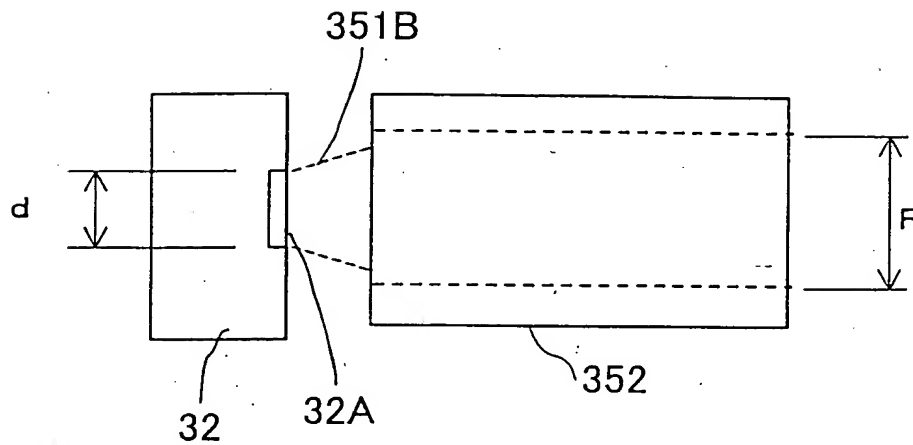


FIG. 100

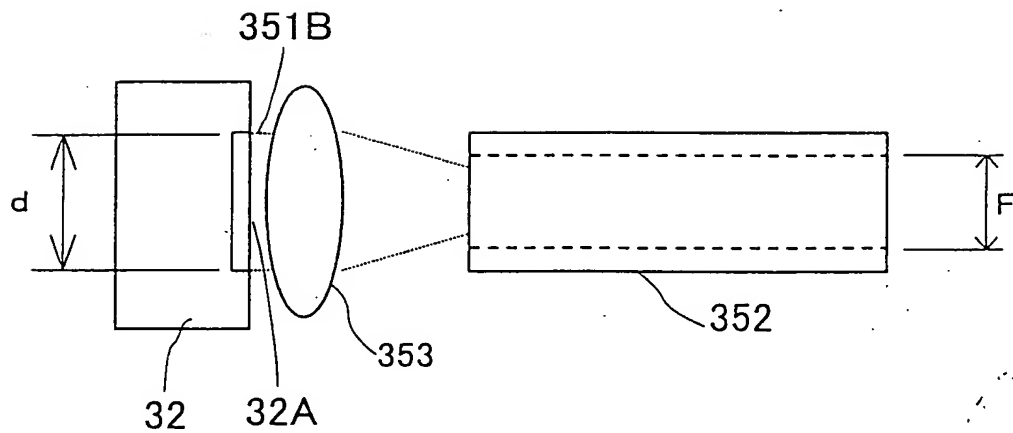


FIG. 101

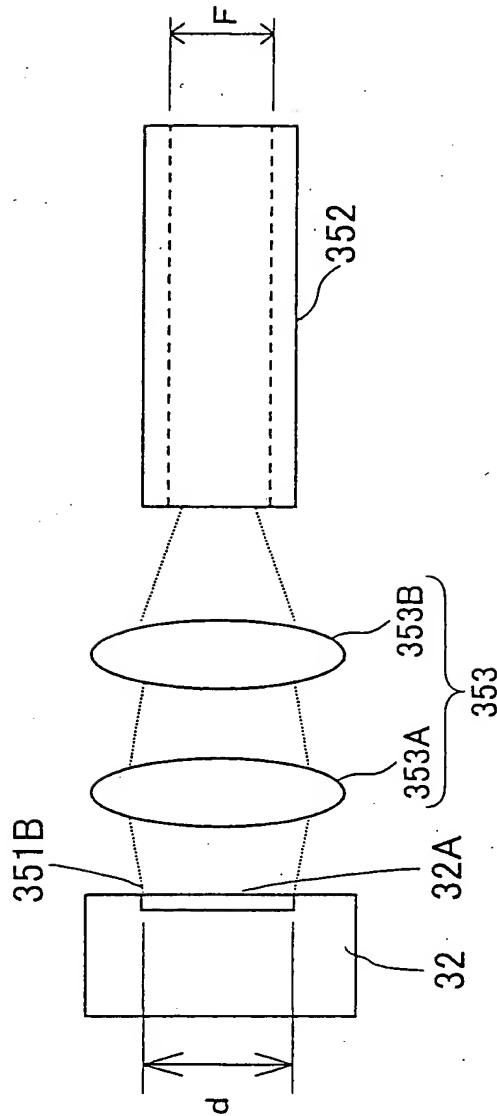


FIG. 102

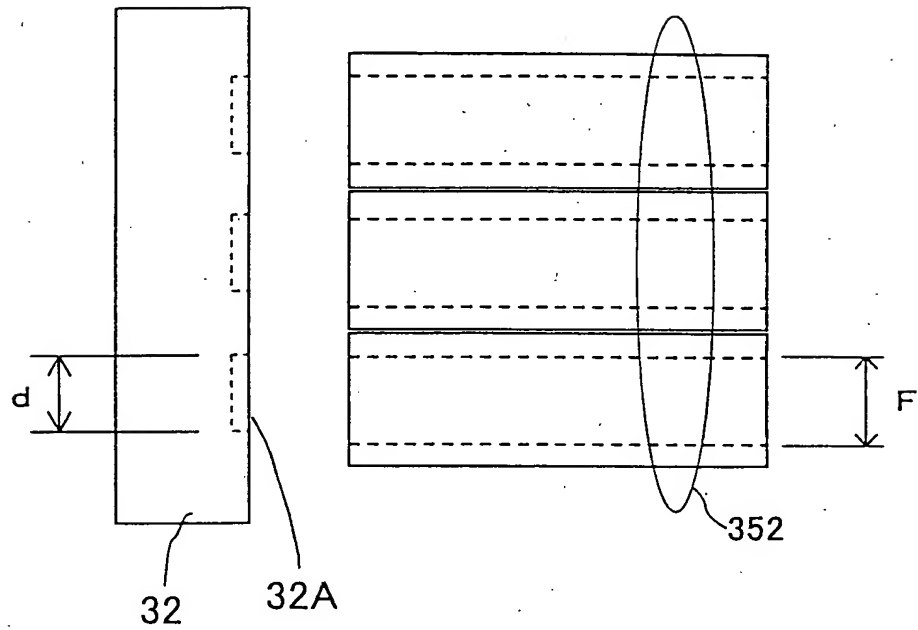


FIG. 103

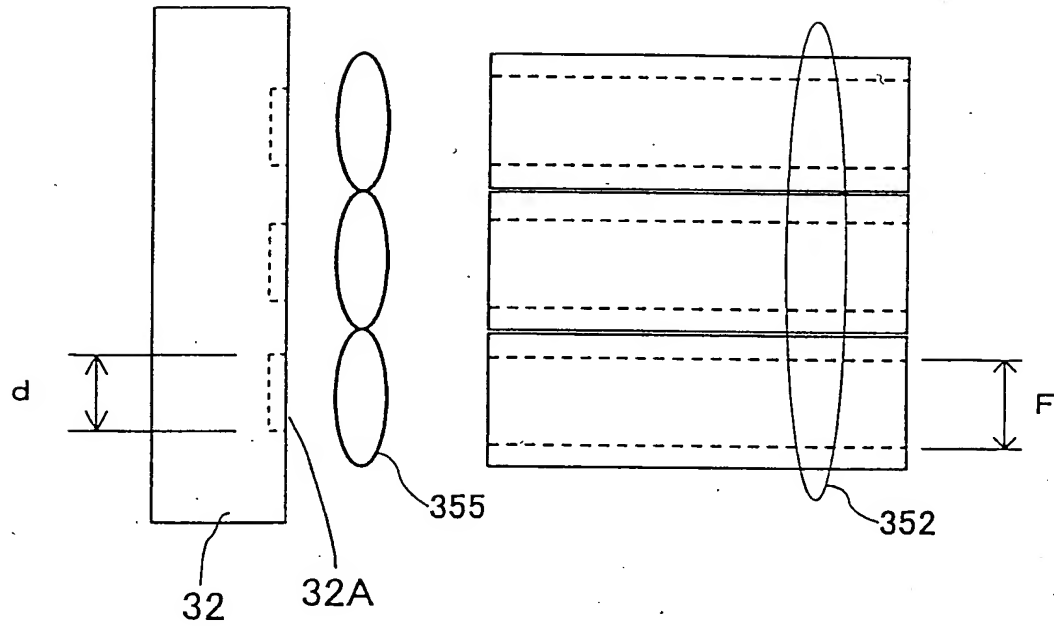




FIG. 104A

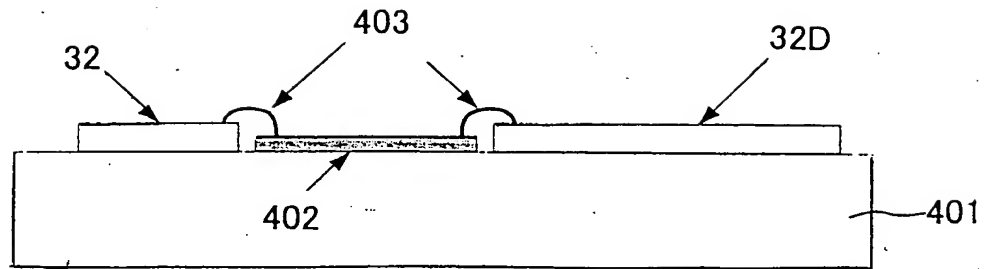


FIG. 104B

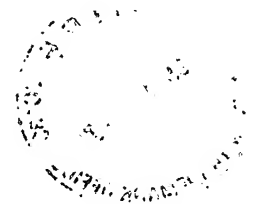
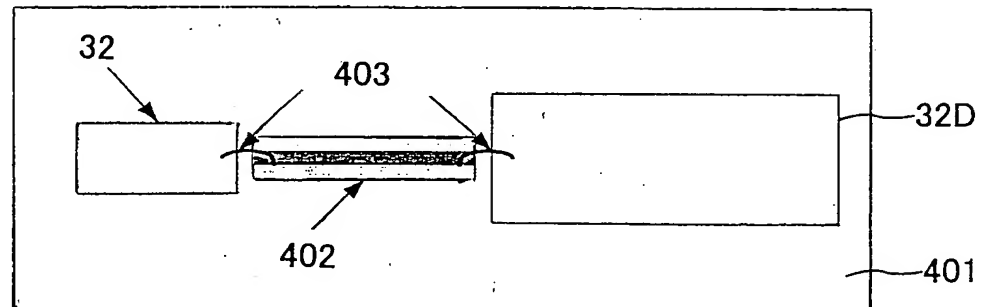
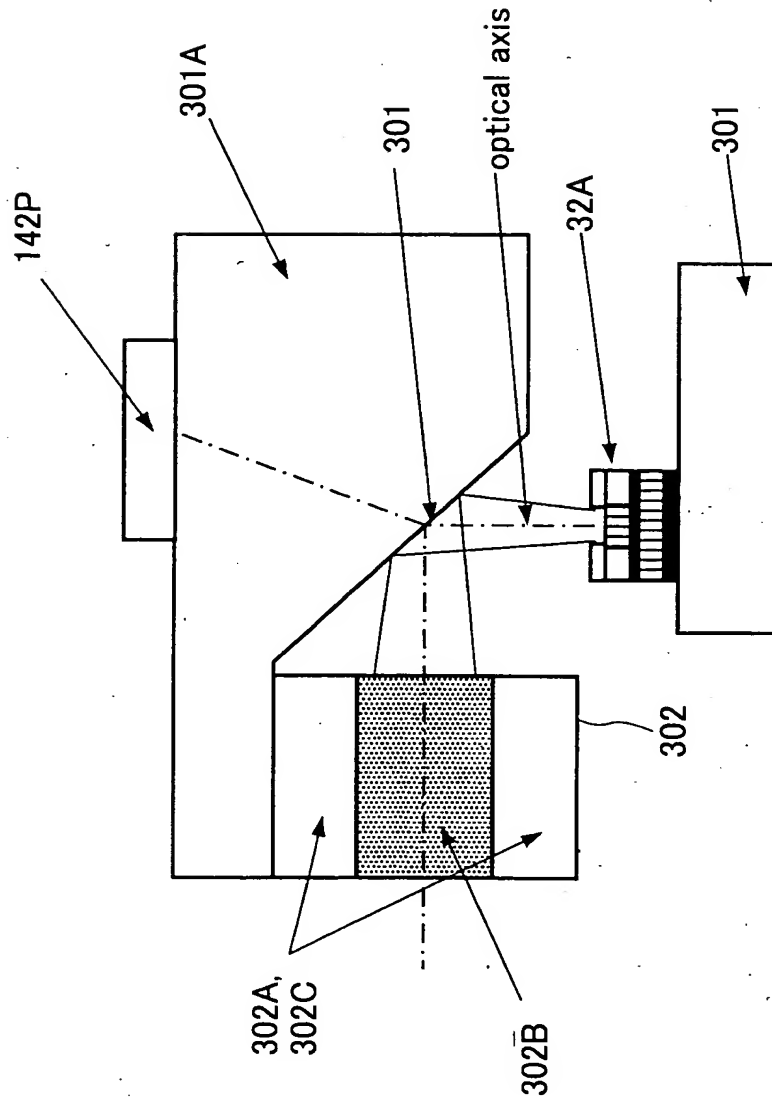


FIG.105



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FIG.106

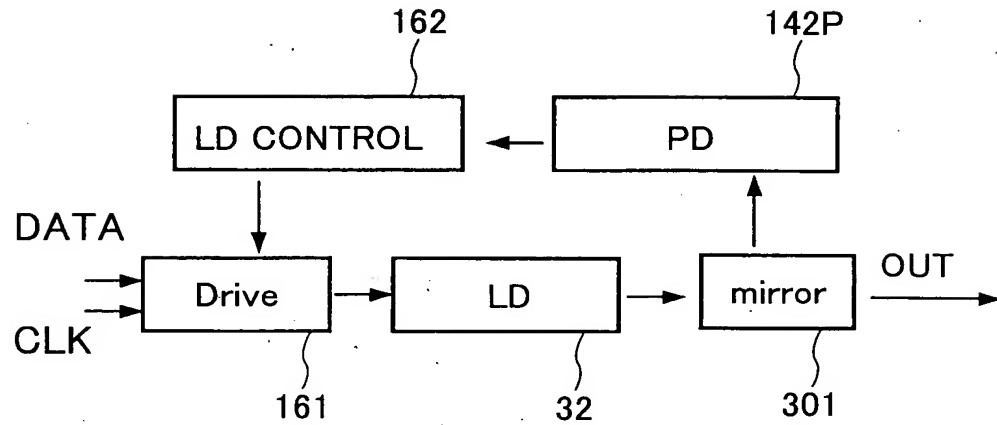


FIG.107

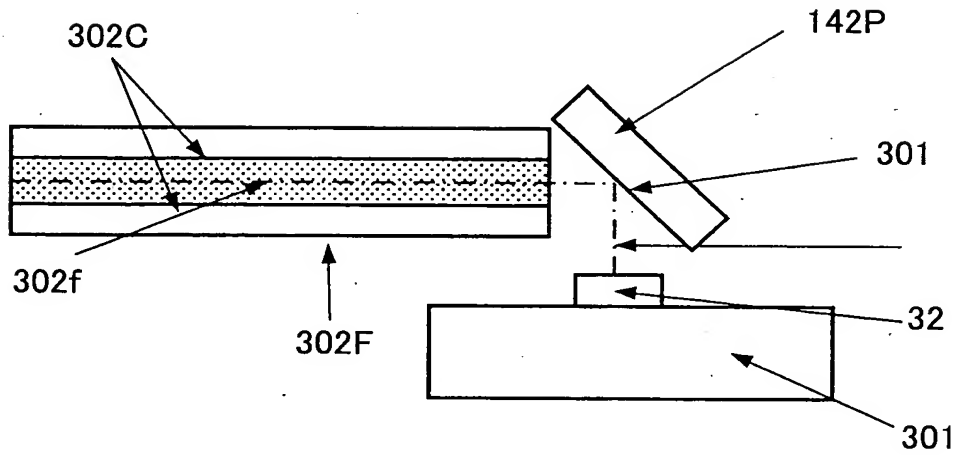


FIG.108

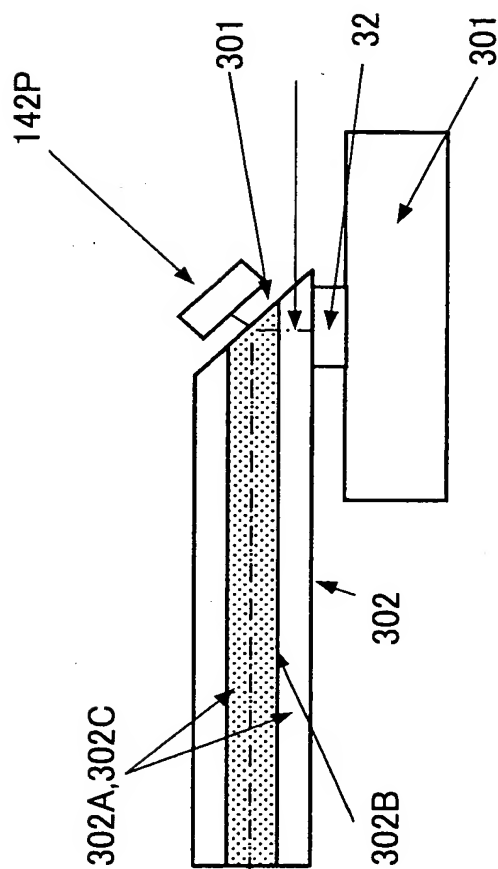


FIG.109

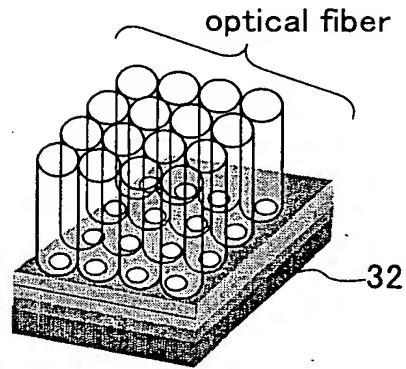


FIG.110A

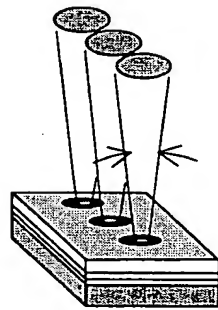


FIG.110B

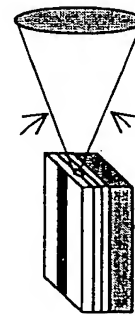


FIG.111A

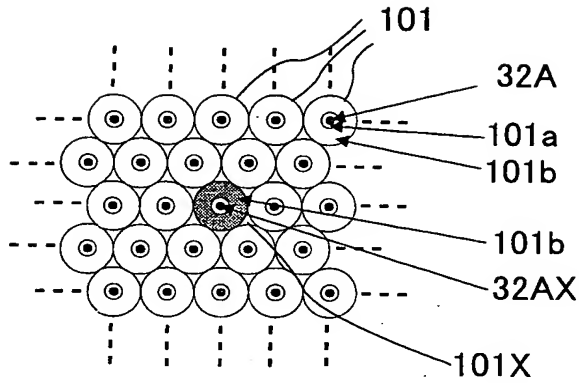


FIG.111B

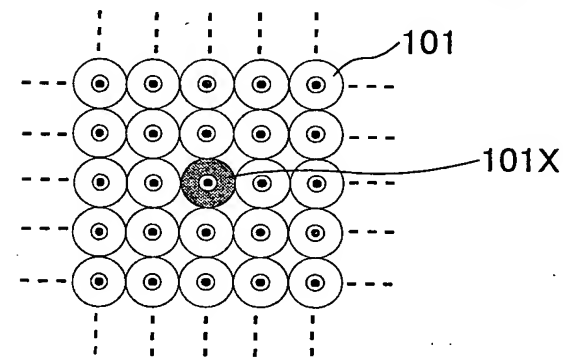


FIG.111C

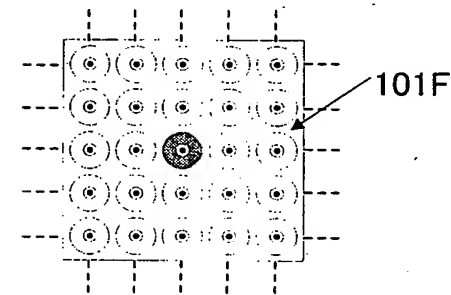


FIG.112

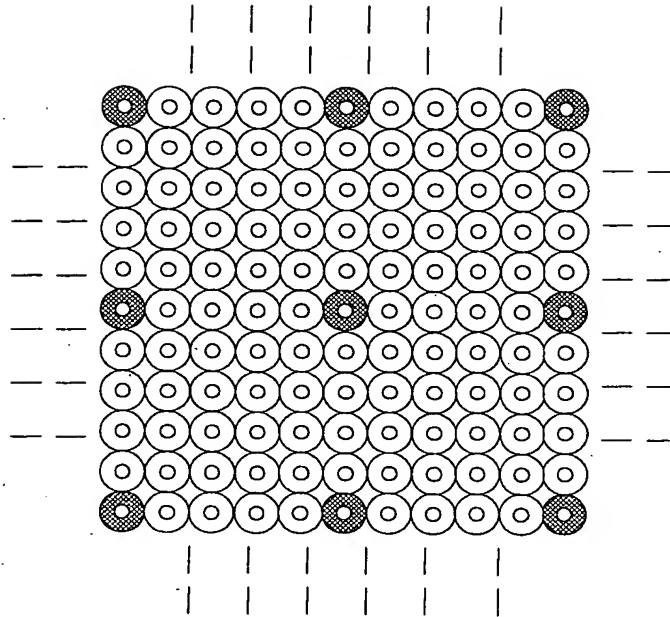




FIG.113B

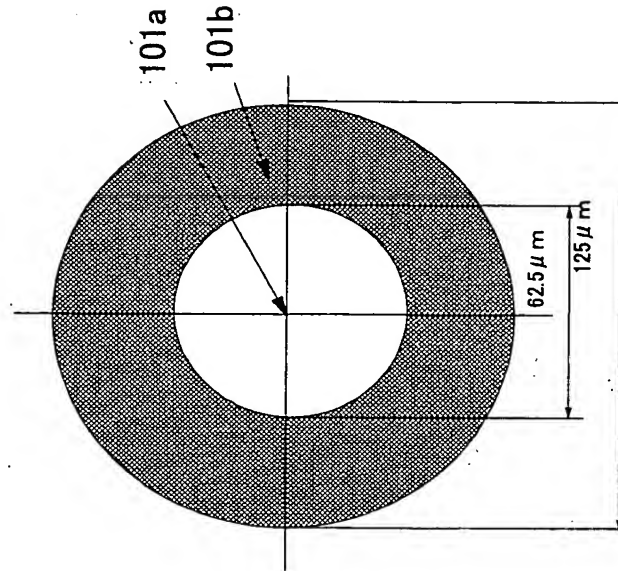


FIG.113A

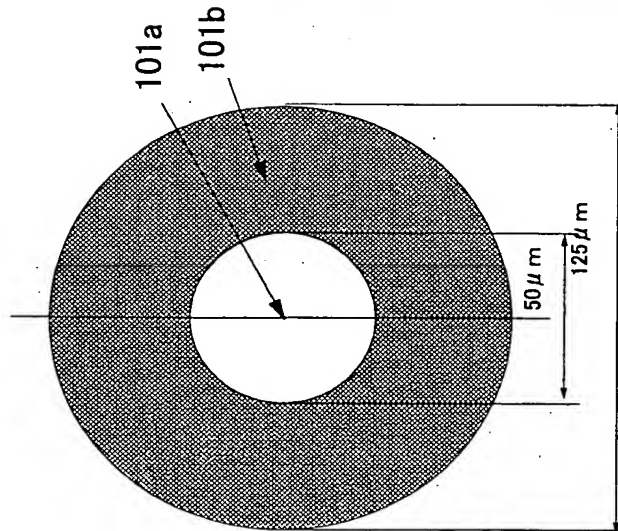


FIG.114

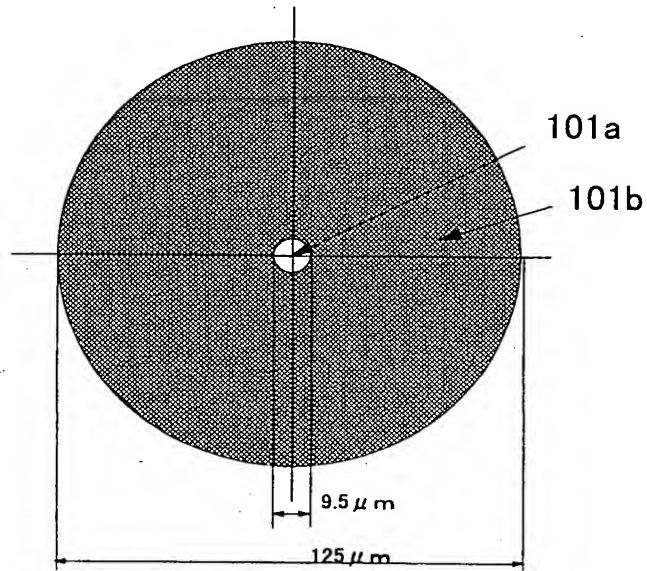


FIG.115

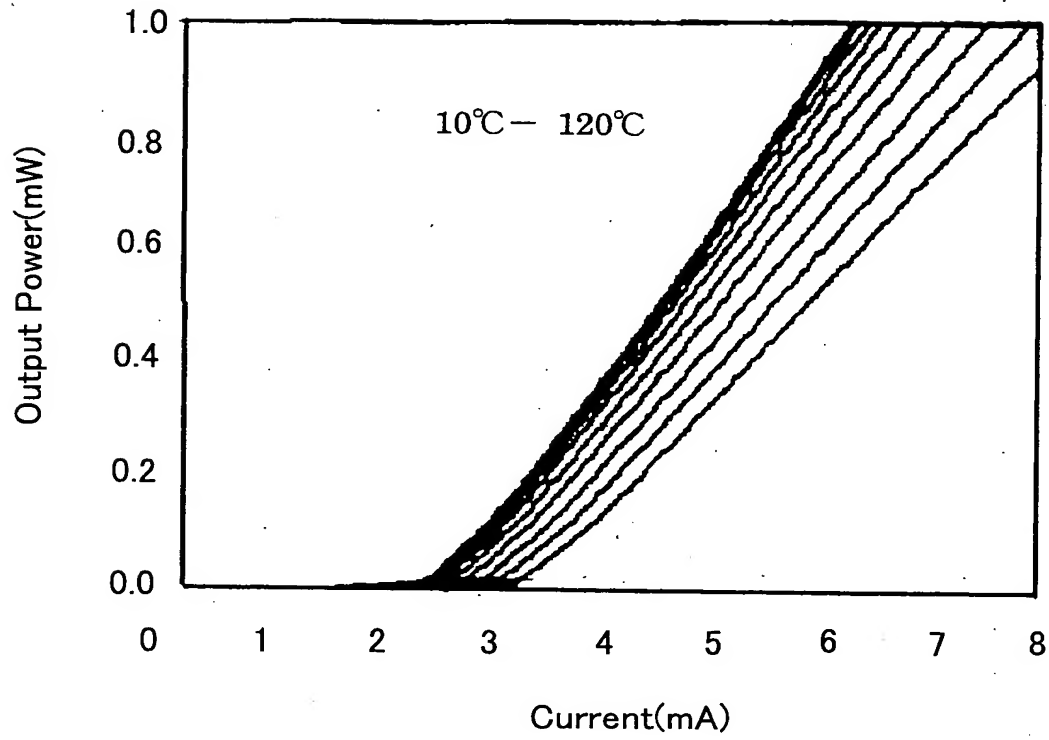


FIG.116

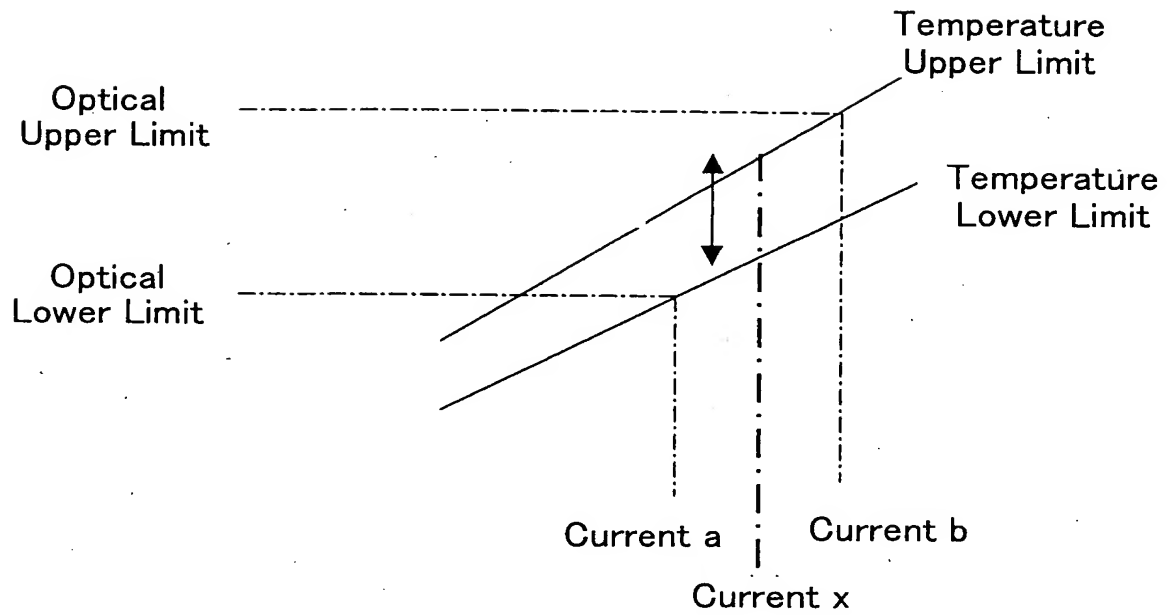


FIG.117

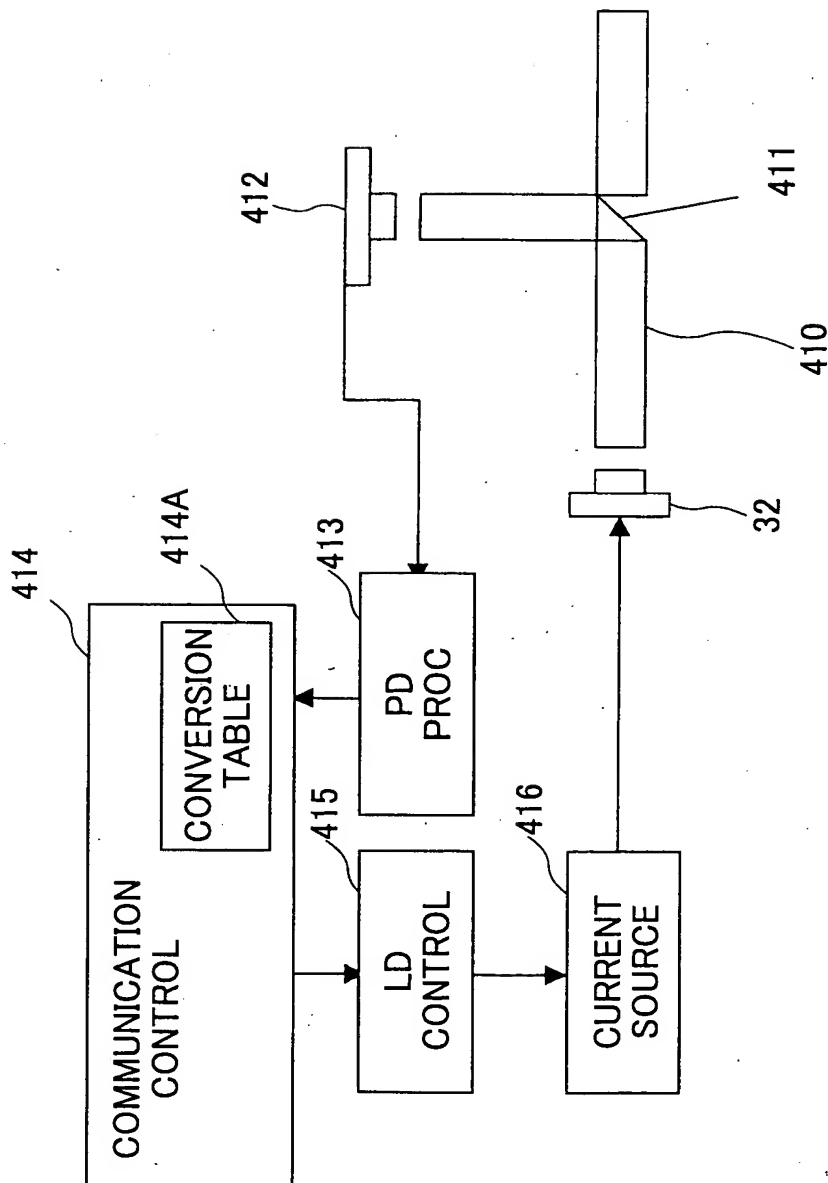


FIG.118

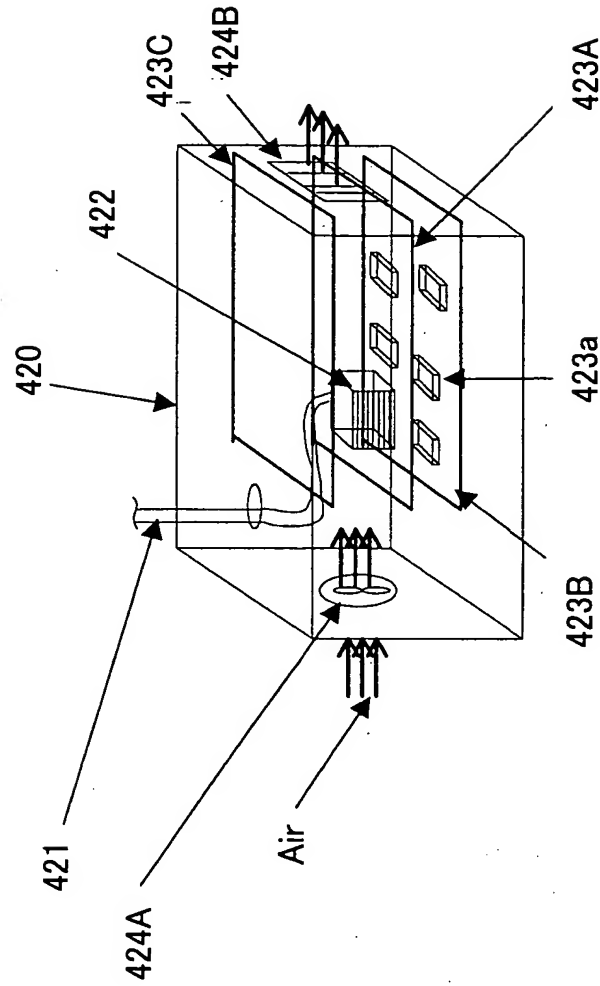


FIG.119

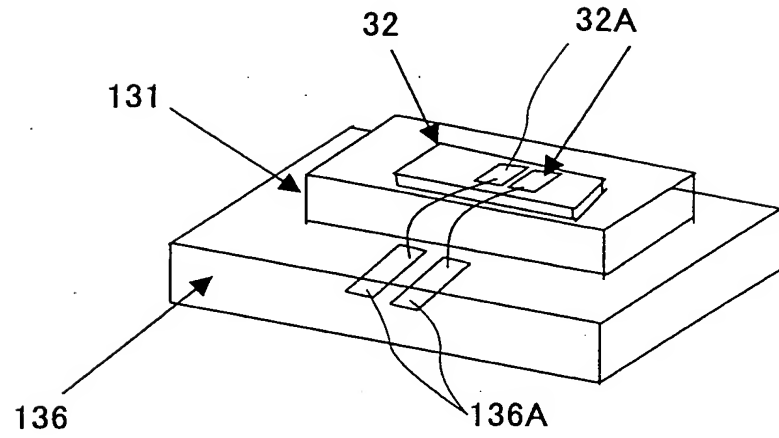


FIG.120

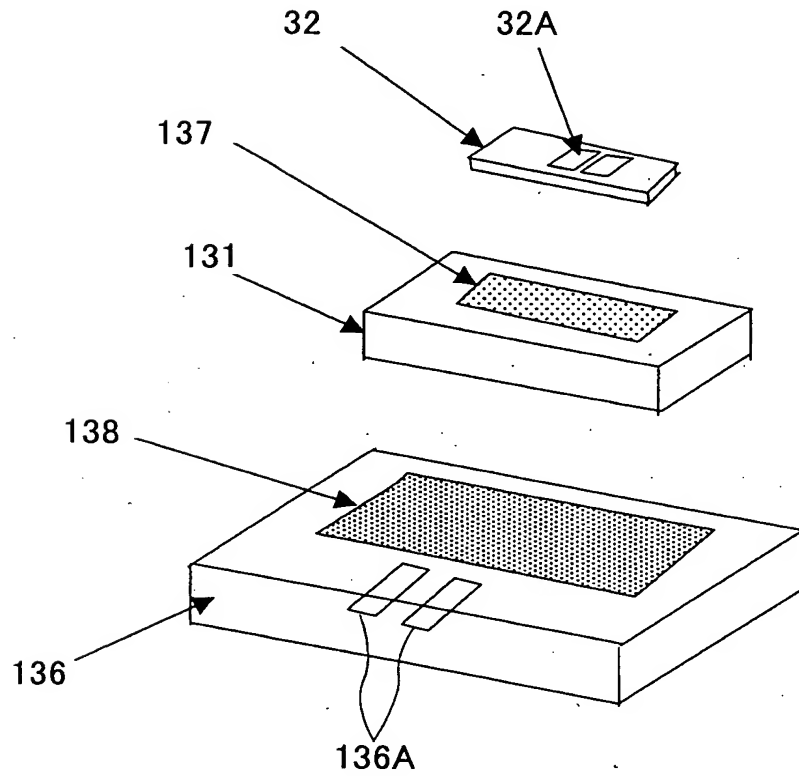




FIG.121

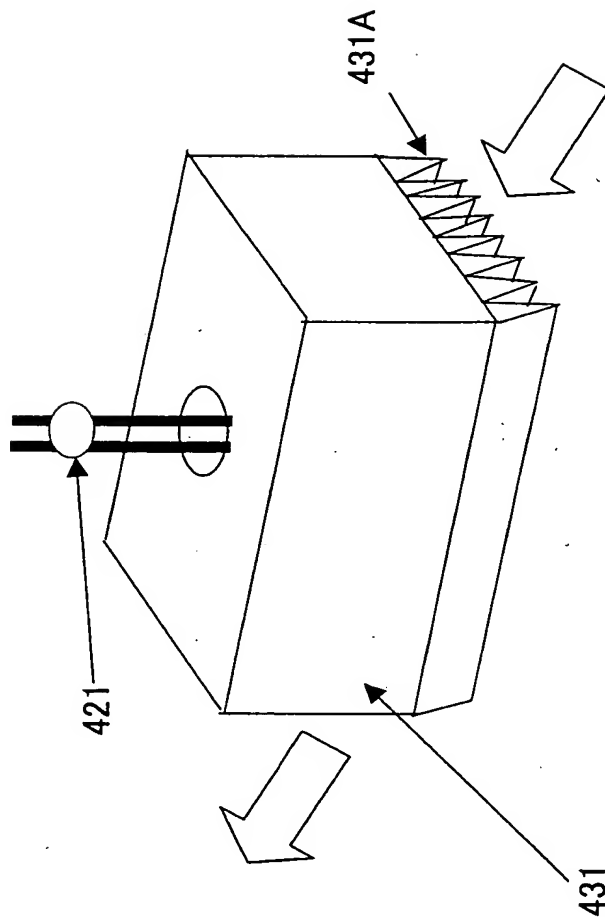


FIG.122

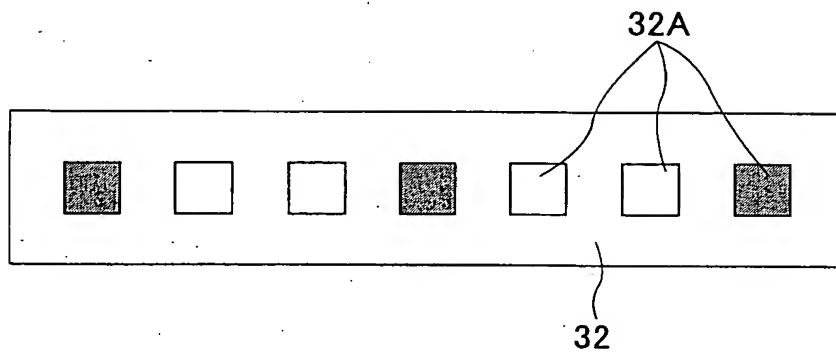
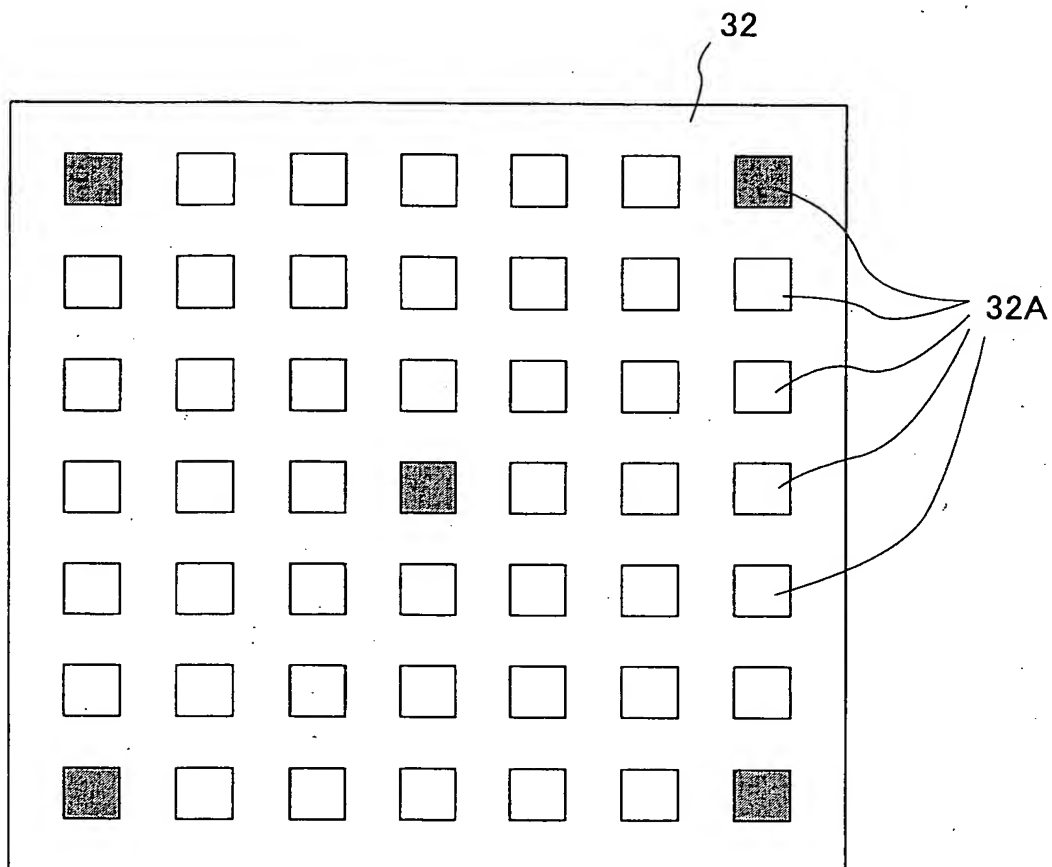


FIG.123



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FIG.124

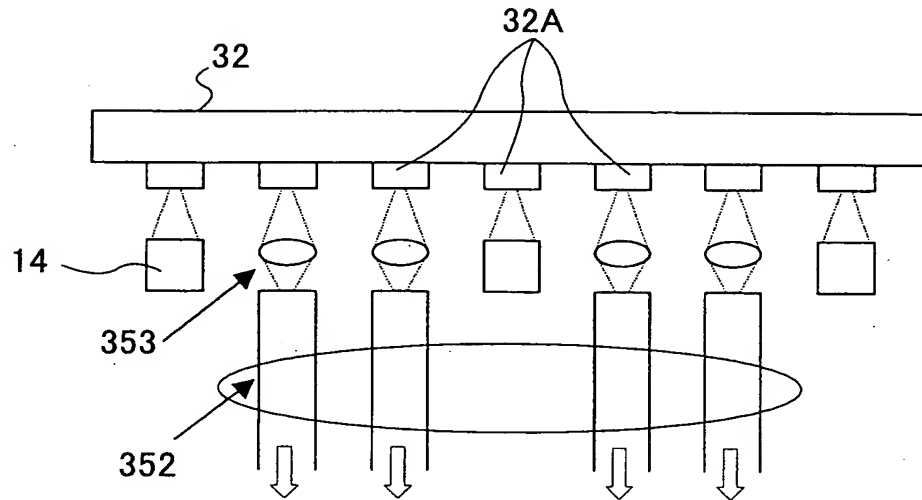


FIG.125

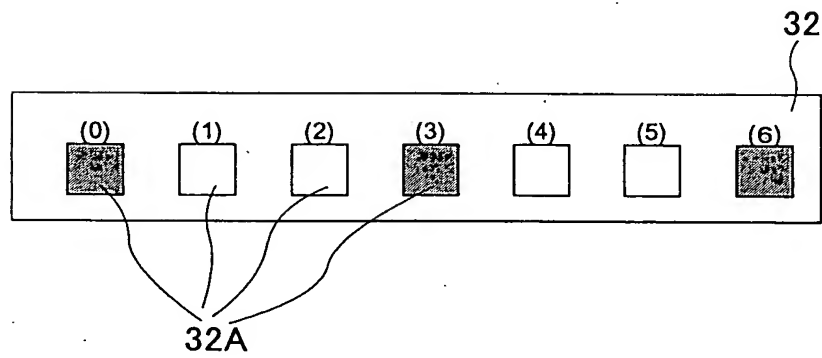


FIG.126

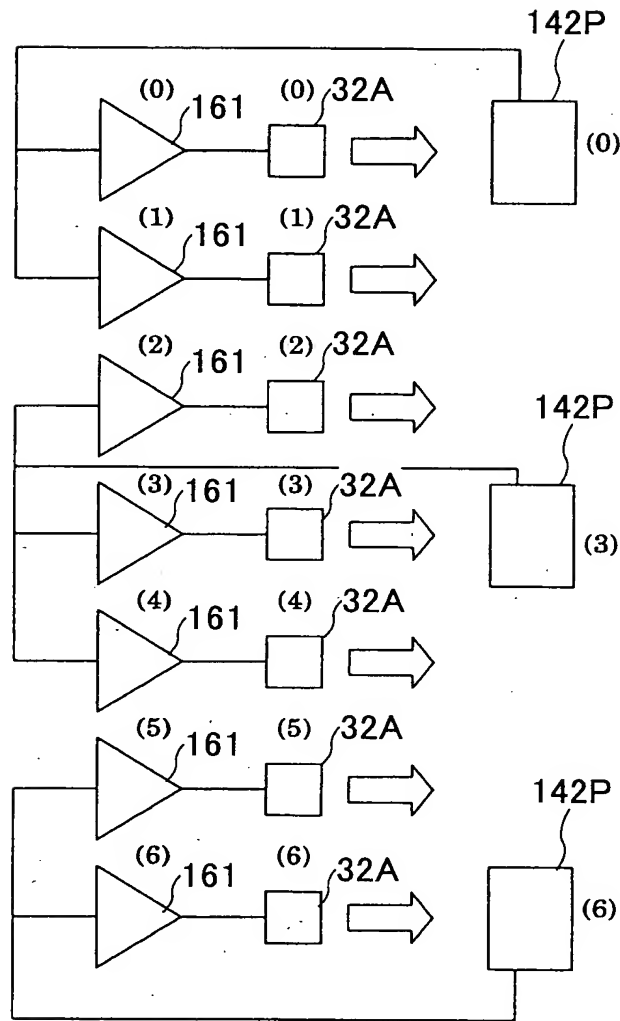


FIG.127

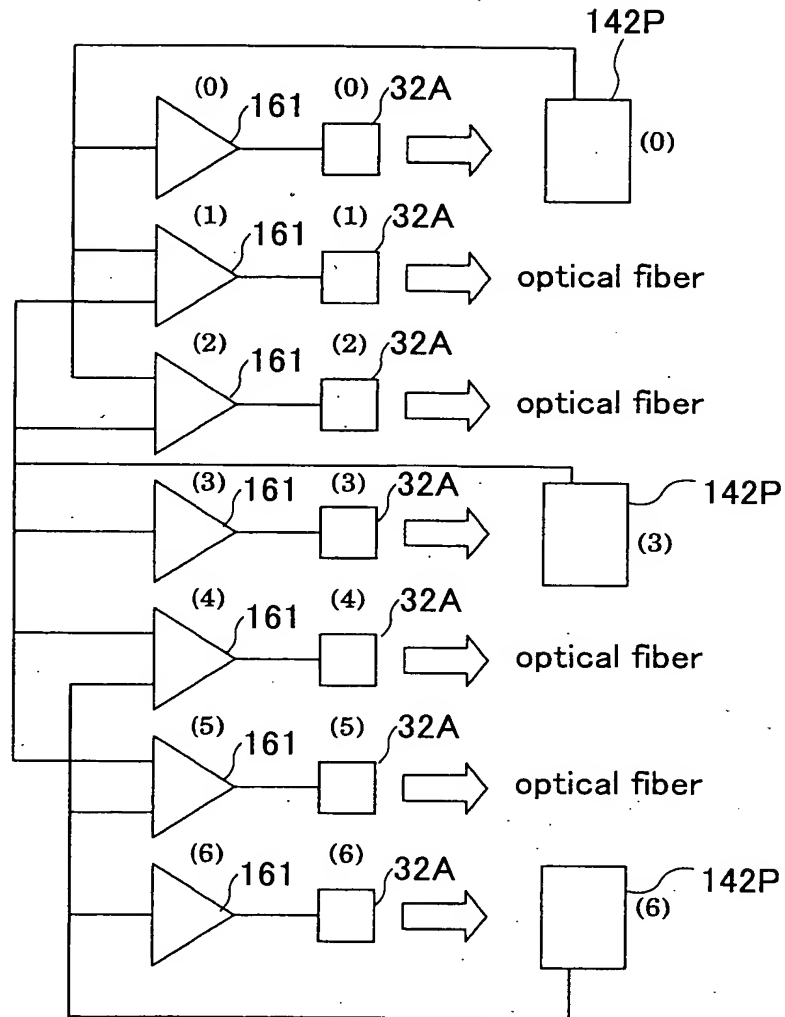


FIG.128

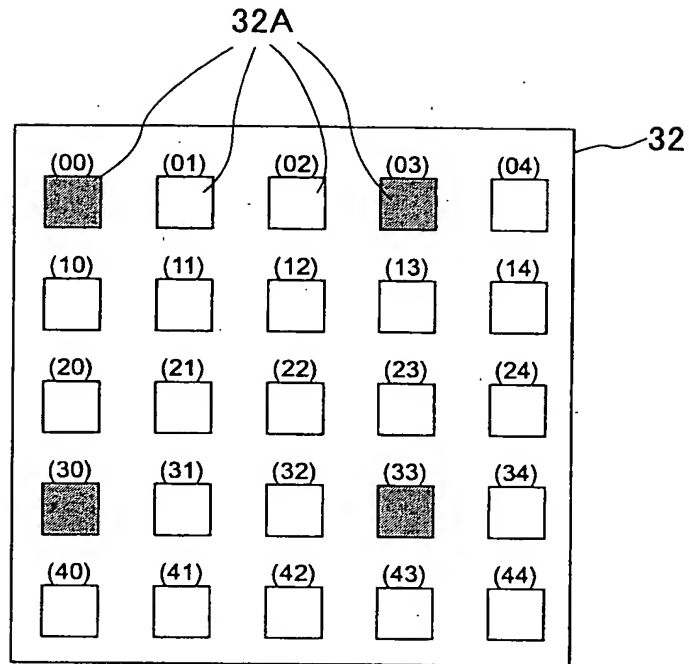


FIG.129

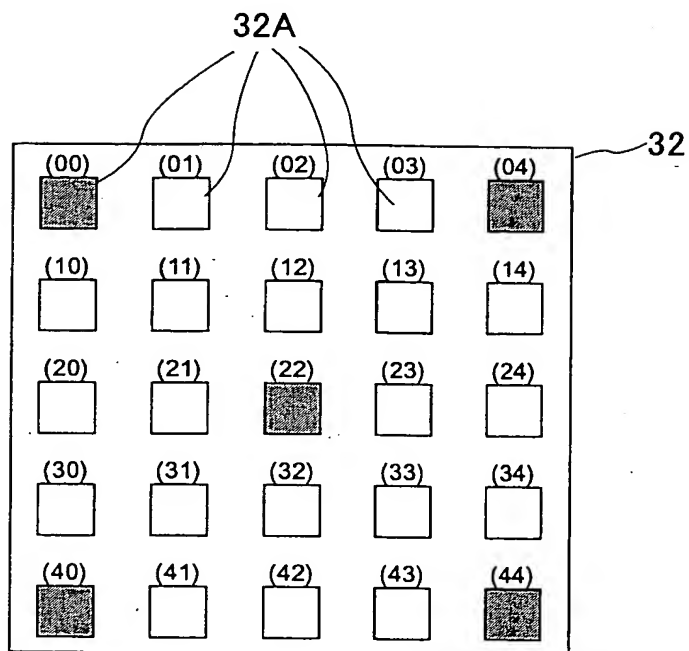




FIG.130

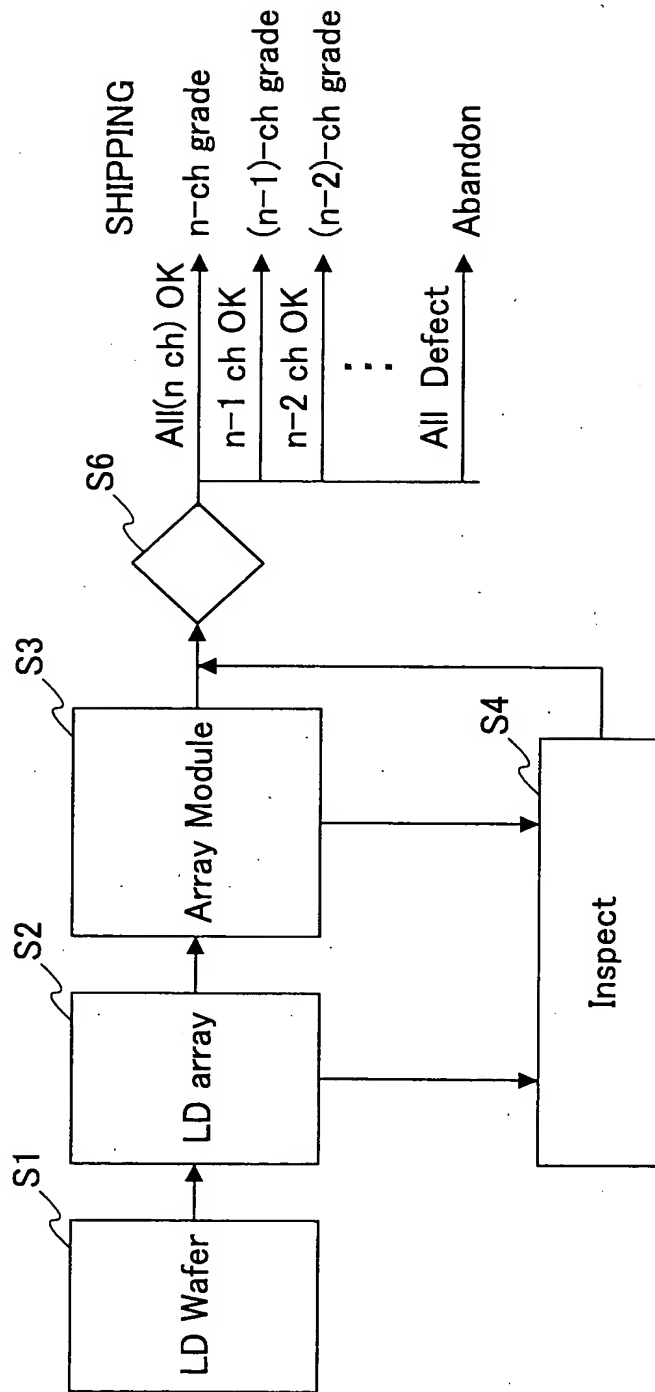


FIG.131

